PN547/C2 VFBGA

Near Field Communication (NFC) controller

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Product data sheet
COMPANY CONFIDENTIAL

1. Introduction

This product data sheet describes PN547/C2, NXP Semiconductors third-generation NFC controller in VFBGA package. This data sheet requires additional documents for functional chip description and design in. Refer to the references listed in this document for full list of documentation provided by NXP.

2. General description

PN547/C2 is a full feature NFC controller designed for integration in mobile devices and devices compliant with NFC standards (NFC Forum, NCI, EMVCo, ETSI/SCP).

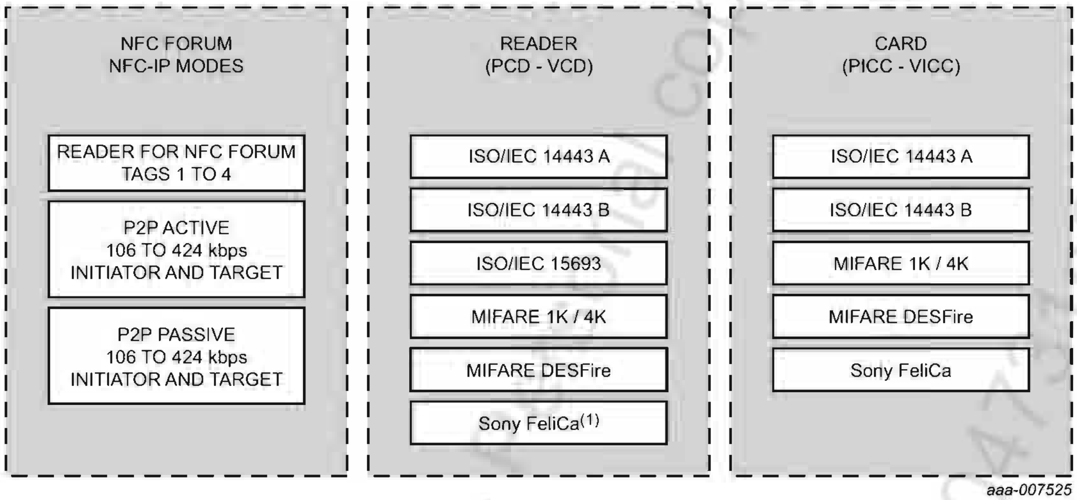
PN547/C2 is designed based on learnings from previous NXP NFC device generation to ease the integration of NFC technology in mobile devices by providing:

- A low PCB footprint and a reduced external Bill of Material by enabling as unique feature the capability to achieve RF standards (NFC Forum, EMVCo card) with small form factor antenna
- An optimized architecture for low-power consumption in different modes (Standby, low-power polling loop)
- A highly efficient integrated power management unit allowing direct supply from a mobile battery for extended battery supply range (2.3 V to 5.5 V) can be achieved. Moreover, this power management provides full flexibility to support the different configurations in the mobile devices (phone ON, phone OFF)

PN547/C2 embeds a new generation RF contactless front-end supporting various transmission modes according to NFCIP-1 and NFCIP-2, ISO/IEC 14443, ISO/IEC 15693, ISO/IEC 18000-3, MIFARE and FeliCa specifications. This new contactless front-end design brings a major performance step-up with on one hand a higher sensitivity and on the other hand the capability to work in active load modulation communication enabling the support of small antenna form factor.

Supported transmission modes are listed in Figure 1. For contactless card functionality, the PN547/C2 can act autonomously if previously configured by the host in such a manner. PICC functionality can be supported without phone being turned on or even with phone battery removed.

PN547/C2 provides a versatile architecture supporting several Secure Element interfaces (2 SWP) allowing a full flexibility for the support of UICC based, microSD based or integrated Secure Element. On top, it enables dynamic multiple Secure Element management (AID routing table).



(1) According to ISO/IEC 18092 (Ecma 340) standard.

Fig 1. PN547/C2 transmission modes

3. Features and benefits

- ARM Cortex M0 microcontroller core
  - Code memory: 96 kB ROM, 28 kB EEPROM
  - Data memory: 7 kB SRAM, 4 kB EEPROM
- Highly integrated demodulator and decoder
- Buffered output drivers to connect an antenna with minimum number of external components
- Integrated RF level detector
- Integrated configurable polling loop for automatic device discovery
- RF protocols supported
  - ISO/IEC 14443A, ISO/IEC 14443B PCD designed according to NFC Forum digital protocol T4T platform and ISO-DEP
  - FeliCa PCD mode
  - MIFARE PCD encryption mechanism (MIFARE 1K and 4K)
  - NFC Forum tag (MIFARE Ultralight, Jewel, Open FeliCa tag, DESFire)
  - ISO/IEC 15693/ICODE VCD mode
  - NFCIP-1, NFCIP-2 protocol
  - ISO/IEC 14443A, ISO/IEC 14443B PICC mode designed according to EMVco PICC
  - FeliCa PICC mode
  - MIFARE PICC mode
- Supported host interfaces
  - NCI protocol interface according to NFC Forum NCI 1.0 standardization
  - SPI-bus
  - I^2C-bus High-speed mode
- Supported Secure Element interfaces

- HCI protocol interfaces according to ETSI/SCP standardization Release 9
- 1 Single Wire Protocol (SWP) interface according to ETSI/SCP standardization Release 9 for UICC connection
- 1 Single Wire Protocol (SWP) interface for additional Secure Element connection (embedded SE or microSD)

- Flexible clock supply concept to facilitate PN547/C2 integration
  - Internal oscillator for 27.12 MHz crystal connection
  - Integrated PLL unit to make use of mobile device reference clock and facilitate PN547/C2 integration
- Integrated power management unit
  - Direct connection to a mobile battery (2.3 V to 5.5 V voltage supply range)
  - 2 power regulators for secure companion chips
  - Support different Hard Power-Down/Standby states activated by firmware
  - Autonomous mode when host is shut down
- Automatic wake-up via RF field, internal timer, SWP and host control interfaces
- Integrated low-power polling loop to allow enabling all technologies in parallel without host interaction
- Integrated non-volatile memory to store data and executable code for customization
- Integrated SWP self tests for production tests
- Standards compliancy
  - EMVCo 2.0.1 for PICC and PCD mode
  - NFC Forum Wave 1 and Wave 2
  - ETSI/SCP 102 613 and 102 622 for SWP/HCI (see Ref. 1 and Ref. 2)

4. Applications

- Mobile devices
- Portable equipment (Personal Digital Assistants, tablet, notebooks)
- Consumer devices

5. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	Card Emulation and Passive Target	2.3	-	5.5	V
V_{BAT}	battery supply voltage	Reader, Initiator and Active target (including 400 mV voltage drop due to the GSM burst)	2.5	-	5.5	V
PV_{DD}	pad power supply (for host interface)	1.8 V host supply	1.65	1.8	1.95	V
PV_{DD}	pad power supply (for host interface)	3 V host supply	2.7	3	3.3	V
SV_{DD}	supply voltage for secure chip interface		1.65	1.8	1.95	V
$SIMV_{CC}$	UICC supply output voltage	no input signal on PMUVCC pin	1.62	1.8	1.98	V
I_{HPD}	Hard Power Down current consumption on VBAT pin	V_{BAT} = 3.6 V; T = 25 °C	-	10.5	12	µA
I_{STBY}	Standby state current consumption on VBAT pin	V_{BAT} = 3.6 V; T = 25 °C	-	-	20	µA
I_{MON}	Monitor state current consumption on VBAT pin	V_{BAT} = 2.75 V; T = 25 °C	-	-	12	µA
I_{LPPOL}	low-power polling loop consumption on VBAT pin	V_{BAT} = 3.6 V; T = 25 °C; loop time = 500 ms	-	150	-	µA
I_{VBAT}	continuous total current consumption	PCD mode at typical 3 V [1]	-	-	170	mA
$I_{SVDD\ max}$	maximum current in Secure Element supply		-	-	20	mA
$I_{TVDDlim}$	current limitation due to embedded limiter in transmitter path	TV_{DD} = 3.1 V [1] [2]	-	180	-	mA
P_{max}	maximum power dissipation	Reader (antenna connected); V_{BAT} = 5.5 V	-	-	550	mW
T_{amb}	operating ambient temperature	JEDEC PCB-0.5	–30	-	+85	°C

[1] The antenna shall be tuned not to exceed the maximum of I_{VBAT}.

[2] This is the threshold of a built-in protection done to limit the current out of TVDD in case of any issue at antenna pins to avoid burning the device. It is not allowed in operational mode to have I_{TVDD} such that I_{VBAT} maximum value is exceeded.

6. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PN5472A2EV/C20803[1][2]	VFBGA49	plastic very thin fine-pitch ball grid array package; 49 balls (I^2C-bus interface)	SOT1320-1
PN5472A2EV/C20804[1][2]	VFBGA49	plastic very thin fine-pitch ball grid array package; 49 balls (SPI-bus interface)	SOT1320-1

[1] Refer to chapter "Licenses".

[2] 0803 and 0804 refer to the EEPROM code version.
The ROM and EEPROM codes functionalities are described in the User Manual document.

7. Marking

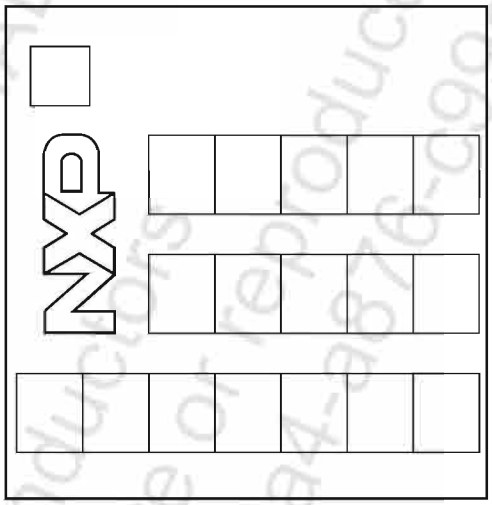


Fig 2. PN547/C2 VFBGA package marking

Table 3. Marking code

Line number	Marking code
Line 1	product version identification
Line 2	diffusion batch sequence number
Line 3	manufacturing code including: • diffusion center code: – Z: SSMC – N: TSMC • assembly center code: – T: APK • RoHS compliancy indicator: – D: Dark Green; fully compliant RoHS and no halogen and antimony • manufacturing year and week, 3 digits: – Y: year – WW: week code • product life cycle status code: – X: means not qualified product – Y: means pre-released product – nothing means released product

8. Block diagram

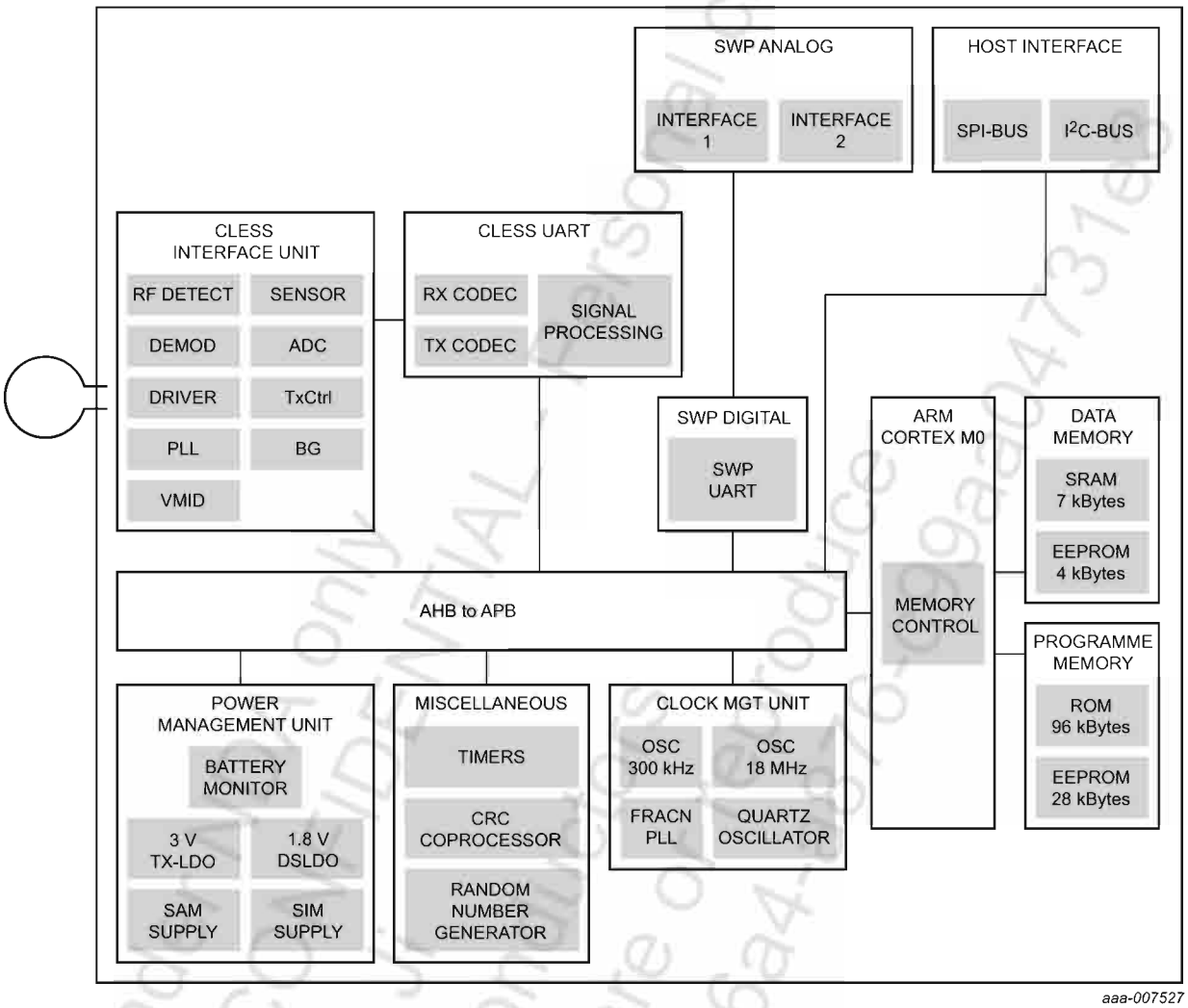


Fig 3. PN547/C2 block diagram

9. Pinning information

9.1 Pinning

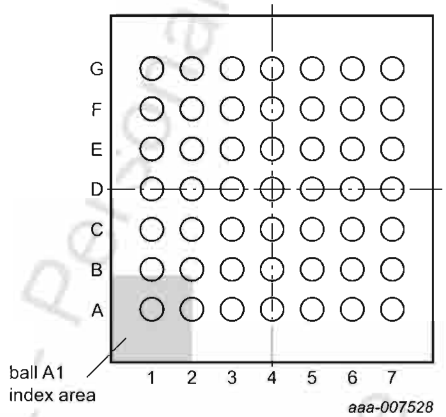


Fig 4. PN547/C2 VFBGA pinning (bottom view)

Table 4. PN547/C2 VFBGA pin description

Symbol	Pin	Type[1]	Refer	Description
DWL_REQ	A1	I	PV_{DD}	firmware download control pin
CLK_REQ	A2	O	PV_{DD}	clock request pin
XTAL1	A3	O	V_{DD}	PLL clock input. Oscillator input
SWIO_UICC	A4	I/O	V_{DD} or $SIMV_{CC}$	SWP data connection to UICC
SIMVCC	A5	P	n/a	power output to supply the UICC
SIGOUT_DWP_TX	A6	O	SV_{DD}	NFC Controller eSE digital transmit signal of SWP
SIGIN_DWP_RX	A7	I	SV_{DD}	NFC Controller eSE digital receive signal of SWP
I2CSCL_SPISCK	B1	I	PV_{DD}	I^2C-bus serial clock input/SPI-bus clock input
I2CADR0_SPINSS	B2	I	PV_{DD}	I^2C-bus address bit0 input/SPI-bus slave select input
PWR_REQ	B3	O	PV_{DD}	power request pin
EXT_SW_CTRL	B4	O	$SIMV_{CC}$	control output signal for external UICC power switch
PMUVCC	B5	P	n/a	UICC power input from external PMU
VSS1	B6	G	n/a	supply ground
SVDD	B7	P	n/a	Secure Element
I2CSDA_SPIMISO	C1	I/O	PV_{DD}	I^2C-bus serial data/SPI-bus data slave output
PVSS	C2	G	n/a	pad ground VSS
XTAL2	C3	I	V_{DD}	oscillator output
VSS	C4	G	n/a	supply ground
RFU2	C5			reserved for future use

Table 4. PN547/C2 VFBGA pin description *…continued*

Symbol	Pin	Type[1]	Refer	Description
VDD	C6	P	n/a	LDO voltage output
VBAT	C7	P	n/a	battery voltage
IRQ	D1	O	PV_{DD}	interrupt request output
I2CADR1_SPIMOSI	D2	I	PV_{DD}	I^2C-bus address bit1 input/SPI-bus slave data input
PVDD	D3	P	n/a	pad supply voltage
VSS2	D4	G	n/a	supply ground
SWIO_SE	D5	IO	SV_{DD}	PN547/C2 SWP master connection to Secure Element
VSS3	D6	G	n/a	supply ground
VDHF	D7	P	n/a	monitor rectifier output voltage
VEN	E1	I	V_{BAT}	reset pin. Set the device in Hard Power Down
DCDC_VSS	E2	G	n/a	supply ground
RFU3	E3			reserved for future use
RFU4	E4			reserved for future use
RFU1	E5			reserved for future use
RFU5	E6			reserved for future use
TVDD	E7	P	n/a	contactless transmitter supply voltage output for decoupling
SAP_DCDC	F1	P	n/a	reserved for future use
SAM_DCDC	F2	P	n/a	reserved for future use
VSS4	F3	G	n/a	supply ground
SMX_7816	F4	O	SV_{DD}	optional connection to SE to indicate if communication is from RF or host interface
RXN	F5	I	V_{DD}	negative receiver Input
RXP	F6	I	V_{DD}	positive receiver Input
VMID	F7	P	n/a	receiver reference voltage input
VBAT2	G1	P	n/a	DC DC connection
VUP	G2	P	n/a	DC DC connection. Supply of TXLDO
TX1	G3	O	TV_{DD}	antenna driver output
TVSS	G4	G	n/a	contactless transmitter ground
TX2	G5	O	TV_{DD}	antenna driver output
ANT2	G6	P	n/a	antenna connection for card emulation
ANT1	G7	P	n/a	antenna connection for card emulation

[1] P = power supply; G = ground; I = input, O = output; I/O = input/output.

9.2 Pin description

In addition to the general pinning list, the pins of PN547/C2 VFBGA can be divided in groups according to the device they are connected to.

Table 5. Host connection pins

Symbol	Pin	Description
VEN	E1	reset pin. Set the device in Hard Power Down
IRQ	D1	interrupt request output
PVDD	D3	pad supply voltage
XTAL1	C3	PLL clock input. Oscillator input
XTAL2	A3	oscillator output
I2CSDA_SPIMISO	C1	I^2C-bus serial data/SPI-bus data slave output
I2CADR0_SPINSS	B2	I^2C-bus address bit0 input/SPI-bus slave select input
I2CADR1_SPIMOSI	D2	I^2C-bus serial clock input/SPI-bus clock input
I2CSCL_SPISCK	B1	I^2C-bus address bit1 input/SPI-bus slave data input
PMUVCC	B5	UICC power input from external PMU
DWL_REQ	A1	firmware download control pin
CLK_REQ	A2	clock request pin
PWR_REQ	B3	power request pin

Table 6. UICC connection pins

Symbol	Pin	Description
SIMVCC	A5	power output to supply the UICC
SWIO_UICC	A4	SWP data connection to UICC
EXT_SW_CTRL	B4	control output signal for external UICC power switch

Table 7. SE connection pins

Symbol	Pin	Description
SVDD	B7	SE power; fixed to SV_{DD} = 1.8 V
SWIO_SE	D5	SWP data connection to Secure Element

Table 8. Antenna connection pins

Symbol	Pin	Description
TX1	G3	antenna driver output
TX2	G5	antenna driver output
RXP	F6	contactless receiver input
RXN	F5	contactless receiver input
VMID	F7	contactless receiver voltage reference
ANT1	G7	antenna connection for Card Emulation
ANT2	G6	antenna connection for Card Emulation

10. Functional description

PN547/C2 can be connected on a host controller through different physical interfaces (I^2C-bus, SPI-bus). The logical interface towards the host baseband is NCI-compliant Ref. 3 with additional command set for NXP-specific product features. This IC is fully user controllable by the firmware interface described in Ref. 9.

PN547/C2 can be connected to a UICC through an SWP interface. Additionally, it provides a second SWP interface towards Secure Element connected via this interface (microSD, embedded Secure Element). Thus, PN547/C2 can provide full Secure Element functionality also without UICC present in the system. The 2 SWP physical interfaces are compliant with ETSI/SCP SWP and HCI, see Ref. 1 and Ref. 2.

Moreover, PN547/C2 provides flexible and integrated power management unit in order to preserve energy supporting Power Off mode. It also allows various power schemes for the UICC.

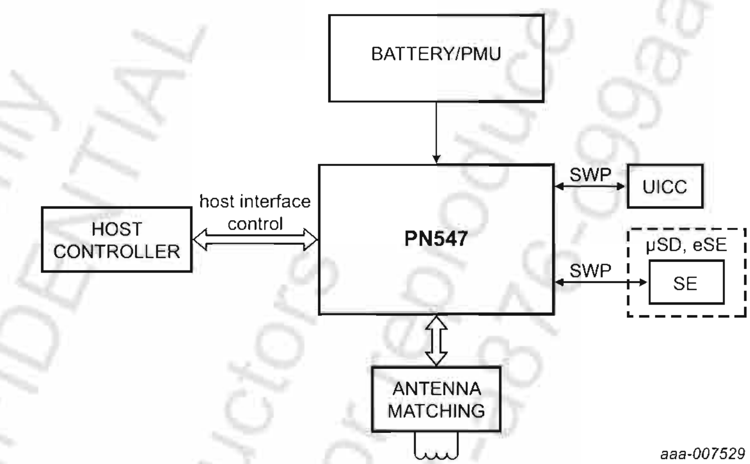


Fig 5. PN547/C2 connection in mobile system

10.1 System modes

10.1.1 System power modes

PN547/C2 is designed in order to enable the different power modes from the system.

3 power modes are specified: Full power mode, Low-power mode and Power Off mode.

Table 9. System power modes description

System power mode	Description
Full power mode	the battery supply (VBAT) as well as the pad supply (PVDD) is available, all use cases can be executed
Low-power mode	the pad supply (PVDD) is not available. Only the Card Emulation mode use cases via SWP are allowed
Power Off mode	the system is not supplied from any source or the system is kept Hard Power Down (HPD)

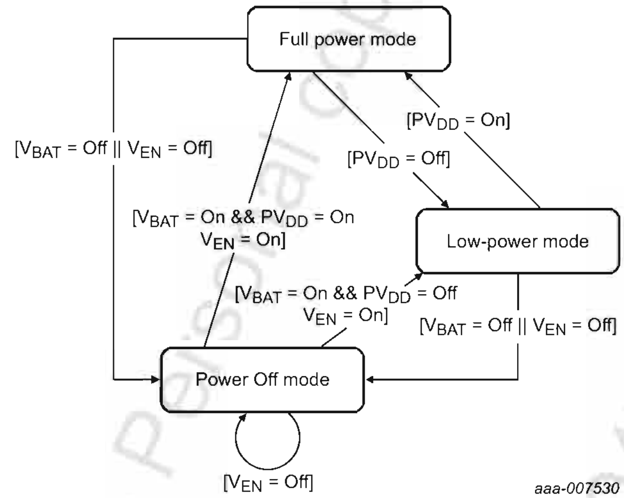


Fig 6. Power mode diagram

Table 10 summarizes the system power mode of the PN547/C2 depending on the status of the external supplies available in the system:

Table 10. Power modes configuration

V_{BAT}	PV_{DD}	V_{EN}	Power mode
Off	Off	X	Power Off mode
Off	On	X	Power Off mode[1]
On	Off	On	Low-power mode
On	X	Off	Power Off mode
On	On	On	Full power mode

[1] Forbidden mode, if $V_{BAT} < PV_{DD}$.

Depending on power modes, some application states are limited:

Table 11. Power modes description

Power mode	Allowed application states
Power Off mode	not applicable
Low-power mode	Card Emulation only
Full power mode	Reader/Writer, Card Emulation, P2P modes

On top of above power modes described, a last power mode «monitor mode» is existing in case of V_{EN} > 1.1 V and battery supply reaching the monitor threshold.

PN547/C2 will autonomously detach internal PMU from battery supply to protect the battery from deep discharge. In monitor mode, PN547/C2 will exit it only if the battery voltage recovers over the critical level. Battery voltage monitor thresholds show hysteresis behavior as defined in Table 31.

10.1.2 PN547/C2 power states

Next to system power modes defined by the status of the power supplies, the power states include the logical status of the system thus extend the power modes.

Four PN547/C2 power states are specified: Monitor, Hard Power Down (HPD), Standby, Active Idle, Active Initiator and Active Target.

Table 12. PN547/C2 power states

Power state Name	Description
Monitor	The PN547/C2 is supplied by VBAT which voltage is below its programmable critical level and the monitor mode is enabled. The system mode is Power Off mode.
Hard Power Down	The PN547/C2 is supplied by VBAT which voltage is above its programmable critical level when monitor mode is enabled and PN547/C2 is kept in Hard Power Down (VEN is kept low by host or SW programming) to have the minimum power consumption. The system mode is in Power Off.
Standby	The PN547/C2 is supplied by VBAT which voltage is above its programmable critical level when the monitor mode is enabled, VEN is high (by host or SW programming) and minimum part of PN547/C2 is kept supplied to enable configured wake-up sources which allow to switch to Active state; RF field, Host interface (if P_{VDD} is high), and SWP. The system mode is Low-power mode or Full power mode.
Active	The PN547/C2 is supplied by VBAT which voltage is above its programmable critical level when monitor mode is enabled, VEN is high (by host or SW programming), PVDD is high and the PN547/C2 internal blocks are supplied. 3 submodes are defined: Idle, Target and Initiator. The system mode is Full power mode.

At application level, the PN547/C2 will continuously switch between different states to optimize the current consumption (polling loop mode). Refer to Table 1 for targeted current consumption in here described states.

The PN547/C2 is designed to allow the host controller to have full control over its functional states, thus of the power consumption of the PN547/C2 based NFC solution and possibility to restrict parts of the PN547/C2 functionality.

10.1.2.1 Monitor state

In monitor mode, the PN547/C2 will exit it only if the battery voltage recovers over the critical level. Battery voltage monitor thresholds show hysteresis behavior as defined in Table 31.

10.1.2.2 Hard Power Down (HPD) state

The Hard Power Down state is entered when PVDD and VBAT are high by setting $V_{EN} < 0.4$ V. As these signals are under host control, the PN547/C2 has no influence on entering or exiting this state.

10.1.2.3 Standby state

Active state is PN547/C2's default state after boot sequence in order to allow a quick configuration of PN547/C2. It is recommended to change the default state to Standby after first boot in order to save power. PN547/C2 can switch to Standby state autonomously (if configured by host). This state is independent of the PVDD value (meaning whatever the state of the mobile device baseband: ON or OFF).

In this state PN547/C2 most blocks including CPU are disconnected from power supply. Number of wake-up sources exist to put PN547/C2 into Active state (all host-related wake-up events imply that PV_{DD} is available):

- Host interface wake-up event (I^2C-bus, SPI-bus)
- Antenna RF level detector
- Internal timer event when using polling loop (380 kHz low-power oscillator is enabled)
- SWP interface

If wake-up event occurs, PN547/C2 will switch to Active state. Any further operation depends on software configuration and/or wake-up source.

10.1.2.4 Active state

Within the Active state, the system is acting as an NFC device. The device can be in 3 different power states: Idle, Initiator and Target.

Table 13. Active power states

Power state name	Description
Idle	the PN547/C2 is active and allows host interface communication as well as SWP communication. The RF interface is not activated.
Target	the PN547/C2 is active and is configured in Target state. The target application can be on a Secure Element or on the host controller.
Initiator	the PN547/C2 is active and is configured in Initiator state. The Initiator state can communicate with a device on the RF interface or with a Secure Element physically connected to the PN547/C2.

Active Initiator state: In this state, PN547/C2 is acting as Reader/Writer or NFC Initiator, searching for or communicating with passive tags or NFC Target. Once RF communication has ended, PN547/C2 will switch to active battery mode (that is, switch off RF transmitter) to save energy. Active Initiator state shall be used with $2.7\ V < V_{BAT} < 5.5\ V$ and $V_{EN} > 1.1\ V$. Active Initiator shall not be used with $V_{BAT} < 2.7\ V$. PV_{DD} is within its operational range (see Table 1).

Active Target state: In this state, PN547/C2 is acting as a card or as an NFC Target. Active Target state shall be used with $2.3\ V < V_{BAT} < 5.5\ V$ and $V_{EN} > 1.1\ V$.

10.1.2.5 Polling loop

The polling loop will sequentially set PN547/C2 in different power states (Active or Standby). All RF technologies withstand by PN547/C2 can be independently enabled within this polling loop.

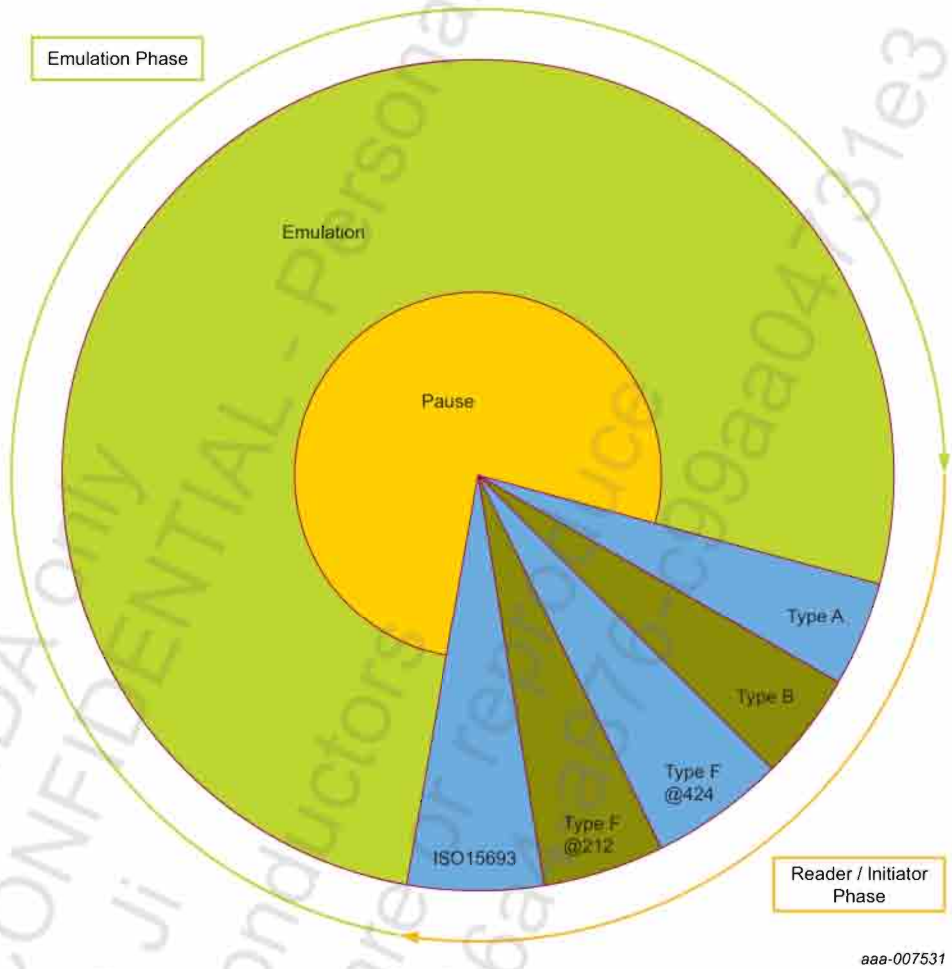


Fig 7. Polling loop: all phases enabled

Emulation phase uses Standby state (when no RF field) and PN547/C2 goes to Target power state when RF field is detected. When in Reader/Initiator phase, PN547/C2 goes to Initiator power state.

To further decrease the power consumption when running the polling loop, PN547/C2 features a low-power RF polling. When at least one of the Initiator states or Reader/Writer modes is enabled, instead of sending regularly RF command PN547/C2 senses with a short RF field duration if there is any target or card/tag present. If yes, then it goes back to standard polling loop. With 500 ms emulation phase duration, the average power consumption is around 150 μA.

Fig 8. Polling loop: low-power RF polling

Detailed description of polling loop configuration options is given in Ref. 9.

10.2 Microcontroller

PN547/C2 is controlled via an embedded ARM Cortex M0 microcontroller core.

The memory organization of PN547/C2 is based on the standard ARM Cortex M0 microcontroller core:

- Code memory: 96 kB ROM, 28 kB EEPROM
- Data memory: 7 kB ROM, 4 kB EEPROM

PN547/C2 features integrated in firmware are referenced in Ref. 9.

10.3 Host interfaces

PN547/C2 provides the support of the following host interfaces:

- SPI-bus Slave Interface, up to 7 MBaud
- I²C-bus Slave Interface, up to 3.4 MBaud

Only one host interface can be active at same time as pins are shared for all interfaces.

The selection between interfaces is fused during IC manufacturing so that different ordering numbers for the I²C-bus, SPI-bus version.

The host interfaces are waken-up in the following way:

- SPI-bus: transition of NSS serial
- I²C-bus: wake-up on I²C-bus address

To enable and ensure data flow control between PN547/C2 and host controller additionally a dedicated interrupt line IRQ is provided which Active state is programmable. See Ref. 9 for more information.

10.3.1 I²C-bus interface

The I²C-bus interface implements a slave I²C-bus interface with integrated shift register, shift timing generation and slave address recognition.

I²C-bus Standard mode (100 kHz SCLK), Fast mode (400 kHz SCLK) and High-speed mode (3.4 MHz SCLK) are supported.

The mains hardware characteristics of the I²C-bus module are:

- Support slave I²C-bus
- Standard, Fast and High-speed modes supported
- Wake-up of PN547/C2 on its address only
- Serial clock synchronization can be used by PN547/C2 as a handshake mechanism to suspend and resume serial transfer (clock stretching)

The I²C-bus interface module meets the I²C-bus specification v03 except General call, 10-bit addressing and Fast mode Plus (Fm+).

10.3.1.1 I²C-bus configuration

- The I²C-bus interface shares four pins with I²C-bus interface also supported by PN547/C2. When I²C-bus is configured in EEPROM settings, functionality of interface pins changes to one described in Table 14.

Table 14. Functionality for I²C-bus interface

Pin name	Functionality
I2CADR0_SPINSS	I²C-bus address 0
I2CADR1_SPIMOSI	I²C-bus address 1
I2CSCL_SPISCK	I²C-bus clock line
I2CSDA_SPIMISO	I²C-bus data line

PN547/C2 supports 7-bit addressing mode. Selection of the I²C-bus address is done by 2-pin configurations on top of a fixed binary header: 0, 1, 0, 1, 0, I2C_ADR1, I2C_ADR0, R/W.

Table 15. I²C-bus interface addressing

I2C_ADR1	I2C_ADR0	I²C-bus address (R/W = 0, write)	I²C-bus address (R/W = 1, read)
0	0	0x50	0x51
0	1	0x52	0x53
1	0	0x54	0x55
1	1	0x56	0x57

10.3.2 Serial Peripheral Interface bus (SPI-bus)

10.3.2.1 Features

- Synchronous, Serial, Full-Duplex communication, 7 MHz max
- Slave mode
- Programmable clock polarity and phase

10.3.2.2 SPI-bus configuration options

In order to select SPI-bus interface for host communication, some EEPROM settings are fused during production.

Four versions can be configured depending on CPOL/CPHA EEPROM setting.

The selection between interfaces is fused during IC manufacturing so that different ordering numbers for the SPI-bus version.

Table 16. SPI-bus configuration

Connection
CPHA switch: Clock PHAse: defines the sampling edge of MOSI data • CPHA = 1: data are sampled on MOSI on the even clock edges of SCK after NSS goes low • CPHA = 0: data are sampled on MOSI on the odd clock edges of SCK after NSS goes low
CPOL switch: Clock POLarity • IFSEL1 = 0: the clock is idle low and the first valid edge of SCK will be a rising one • IFSEL1 = 1: the clock is idle high and the first valid edge of SCK will be a falling one

The SPI-bus interface shares 4 pins with I²C-bus interface also supported by PN547/C2. When SPI-bus is configured in EEPROM settings, functionality of interface pins changes to one described in Table 17.

Table 17. Functionality for SPI-bus interface

Pin name	Functionality
I2CADR0_SPINSS	NSS (Not Slave Select)
I2CADR1_SPIMOSI	MOSI (Master Out Slave In)
I2CSCL_SPISCK	SCK (Serial Clock)
I2CSDA_SPIMISO	MISO (Master In Slave Out)

10.3.2.3 SPI-bus functional description

When a master device transmits data to PN547/C2 (slave device) via the MOSI line, PN547/C2 responds by sending data to the master device via the masters MISO line. This implies full-duplex transmission with both data out and data in synchronized with the same clock signal.

PN547/C2 starts logic when receiving a logic low at pin NSS and the clock at input pin SCK. Thus, PN547/C2 is synchronized with the master. Data from the master is received serially at the slave MOSI line and loads the 8-bit shift register. After the 8-bit shift register is loaded, its data is transferred to the read buffer. During a write cycle, data is written into the shift register, then PN547/C2 waits for a clock train from the master to shift the data out on the slaves MISO line.

- Master In Slave Out (MISO)

  The MISO line is configured as an input in a master device and as an output in a slave device. It is used to transfer data from the slave to the master, with the most significant bit sent first. The MISO line of a slave device should be placed in the high impedance state if the slave is not selected.

- Master Out Slave In (MOSI)

  The MOSI line is configured as an output in a master device and as an input in a slave device. It is used to transfer data from the master to a slave, with the Most Significant Bit (MSB) sent first.

- Serial Clock (SCK)

  The serial clock is used to synchronize data movement both in and out of the device through its MOSI and MISO lines. The master and slave devices are capable of exchanging a byte of information during a sequence of eight clock cycles. Since the master device generates SCK, this line becomes an input on a slave device and an output at the master device.

- Not Slave Select (NSS)

  The slave select input line is used to select a slave device. It has to be low prior to data transactions and must stay low of the duration of the transaction. The NSS line on master side must be tied high.

Both master and slave devices must operate with the same timing. The master device always places data on the MOSI line a half cycle before the clock edge SCK, in order for the slave device to latch the data.

For more information about the SPI-bus functionality see Ref. 8.

10.4 Secure Element interfaces

PN547/C2 supports 2 Single Wire Protocol (SWP) interfaces to be connected to Secure Element.

10.4.1 SWP interface

PN547/C2 features ETSI-compliant SWP interface towards UICC (see Ref. 1).

PN547/C2 supports the ETSI optional CLT mode for MIFARE as well as for FeliCa (see Ref. 1).

The SWP interface is a bit oriented, point-to-point communication protocol between a UICC and the contactless front end, like PN547/C2. PN547/C2 is the master and the UICC is the slave. This interface is based on the transmission of digital information in full-duplex mode. The master sends information on the wire in the voltage domain, while the slave sends information back in the current domain.

PN547/C2 SWP interface implementation features 4 different baud rates:

- 910 kbit/s (activated by embedded FW by default)
- 1.25 Mbit/s (activated by embedded FW if the UICC supports it, otherwise stays at 910 kbit/s)

PN547/C2 also allows configuration of SWIO pin in high impedance state. The application can choose to have PN547/C2 configuring this high impedance automatically when UICC class B is detected, or on demand via host. For the configuration, refer to Ref. 9.

PN547/C2 allows configuration of an external pin PWR_REQ to request the application to provide supply to the UICC. For the configuration, refer to Ref. 9.

Only one SWP HW interface can be active at a time. The switch between the 2 hardware SWP interfaces is managed by the PN547/C2 firmware in a sequential way.

10.5 PN547/C2 clock concept

There are 4 different clock sources in PN547/C2:

- 27.12 MHz clock coming either/or from:
  - Internal oscillator for 27.12 MHz crystal connection
  - Integrated PLL unit which includes a 1 GHz VCO
- 13.56 MHz RF clock recovered from RF field
- Low-power oscillator 10 MHz/20 MHz
- Low-power oscillator 380 kHz

10.5.1 27.12 MHz quartz oscillator

When enabled, the 27.12 MHz quartz oscillator applied to PN547/C2 is the time reference for the RF front end when PN547/C2 is behaving in Reader mode or NFC-DEP Initiator.

Therefore stability of the clock frequency is an important factor for reliable operation. It is recommended to adopt the circuit shown in Figure 9.

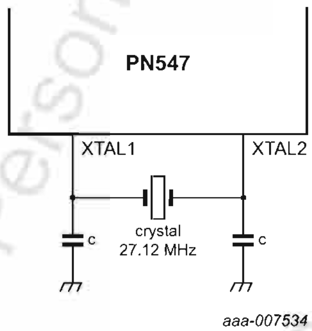


Fig 9. 27.12 MHz crystal oscillator connection

The Table 18 describes the levels of accuracy and stability required on the crystal.

Table 18. Crystal requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CLK}	CLK frequency	ISO/IEC and FCC compliancy	-	27.12	-	MHz
f_{CLK_ACC}	CLK frequency accuracy	full operating range [1]	–100	-	+100	ppm
		all V_{BAT} range Temp = 20°C [1]	–50	-	+50	ppm
		all temperature range V_{BAT} = 3.6 V [1]	–50	-	+50	ppm
ESR	equivalent series resistance		-	50	100	Ω
C_L	load capacitance		-	10	-	pF
P_{CLK}	drive level		-	-	100	µW

[1] This requirement is according to FCC regulations requirements. To meet only ISO/IEC 14443 and ISO/IEC 18092 then ± 14 kHz apply.

10.5.2 Integrated PLL to make use of external clock

When enabled, the PLL is designed to generate a low noise 27.12 MHz for an input clock 13 MHz, 19.2 MHz, 24 MHz, 26 MHz, 38,4 MHz and 52 MHz

The 27.12 MHz output of the PLL is used as the time reference for the RF front end when PN547/C2 is behaving in Reader mode or ISO/IEC 18092 Initiator as well as in Target when configured in Active Communication mode.

The input clock on XTAL1 shall comply with the following phase noise requirements for the following input frequency: 13 MHz, 19.2 MHz, 24 MHz, 26 MHz, 38,4 MHz and 52 MHz:

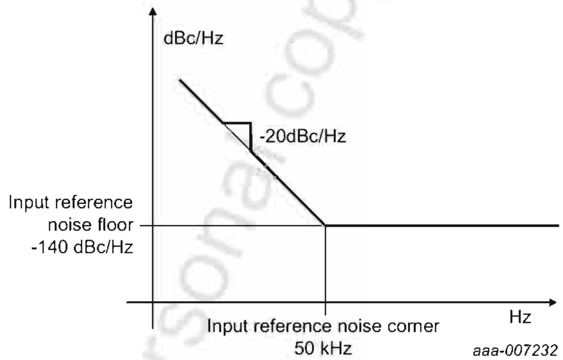


Fig 10. Input reference phase noise characteristics

This phase noise is equivalent to an RMS jitter of 6.23 ps from 10 Hz to 1 MHz. For configuration of input frequency, refer to Ref. 9. There are 6 pre programmed and validated frequency for the PLL: 13 MHz, 19.2 MHz, 24 MHz, 26 MHz, 38.4 MHz and 52 MHz.

Table 19. PLL input requirements

Coupling: single-ended, AC coupling;

Parameter	Conditions		Min	Typ	Max	Unit
input frequency	ISO/IEC and FCC compliancy		-	13	-	MHz
			-	19.2	-	MHz
			-	24	-	MHz
			-	26	-	MHz
			-	38.4	-	MHz
			-	52	-	MHz
frequency accuracy	full operating range; frequencies typical values: 13 MHz, 26 MHz and 52 MHz	[1]	–25	-	+25	ppm
	full operating range; frequencies typical values: 19.2 MHz, 24 MHz and 38.4 MHz	[1]	–50	-	+50	ppm
phase noise requirement	input noise floor at 50 kHz		–140	-	-	dB/Hz
Sinusoidal shape						
amplitude peak to peak			0.2	-	1.8	V
voltage			0	-	1.8	V
Square shape						
voltage			0	-	1.8 ± 10%	V

[1] This requirement is according to FCC regulations requirements. To meet only ISO/IEC 14443 and ISO/IEC 18092 then ± 400 ppm limits apply.

For detailed description of clock request mechanisms refer to Ref. 9 and Ref. 10.

10.5.3 Low-power 20 MHz oscillator

Low-power 20 MHz oscillator is used as system clock of the system.

10.5.4 Low-power 380 kHz oscillator

A Low Frequency Oscillator (LFO) is implemented to drive a counter (WUC) waking-up PN547/C2 from Standby state. This allows implementation of low-power reader polling loop at application level. Moreover, this 380 kHz is used as the reference clock for write access to EEPROM memory.

10.6 Power concept

10.6.1 PMU functional description

The Power Management Unit of PN547/C2 generates internal supplies required by PN547/C2 out of V_{BAT} or V_{PMUVCC} inputs supplies:

- V_{DD}: analog supply
- DV_{DD}: digital supply
- TV_{DD}: supply for RF transmitter
- SV_{DD}: supply of the Secure Element connected
- $SIMV_{CC}$: supply of the UICC when its power input is not directly connected to the mobile PMU

Figure 11 describes the main blocks available in PMU:

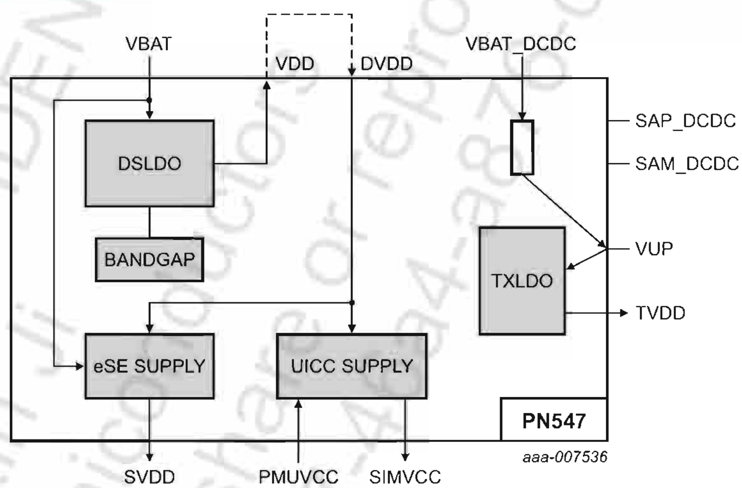


Fig 11. PMU functional diagram

10.6.2 Dual supply LDO (DSLDO)

The input pin of the DSLDO is VBAT.

The low drop-out regulator provides V_{DD} (analog supply) required in PN547/C2.

V_{DD} (analog supply) shall be connected externally to DV_{DD} (digital core supply).

10.6.3 TXLDO

This is the LDO which generates the transmitter voltage.

The value of TV_{DD} is configured at 3.1 V ± 0.2 V.

TV_{DD} value is given according to the minimum targeted V_{BAT} value for which Reader mode shall work.

For V_{BAT} above 3.1 V, TV_{DD} = 3.1 V:

$$V_{BAT} \geq 3.1 \Rightarrow TV_{DD} = 3.1V$$

$$3.1V > V_{BAT} \geq 2.3V \Rightarrow TV_{DD} = V_{BAT}$$

In Standby state, TV_{DD} is around 2.5 V with some ripples; it toggles between 2.35 V to 2.65 V with a period which depends on the capacitance and load on TVDD.

Figure 12 shows TV_{DD} behavior for3.1 V:

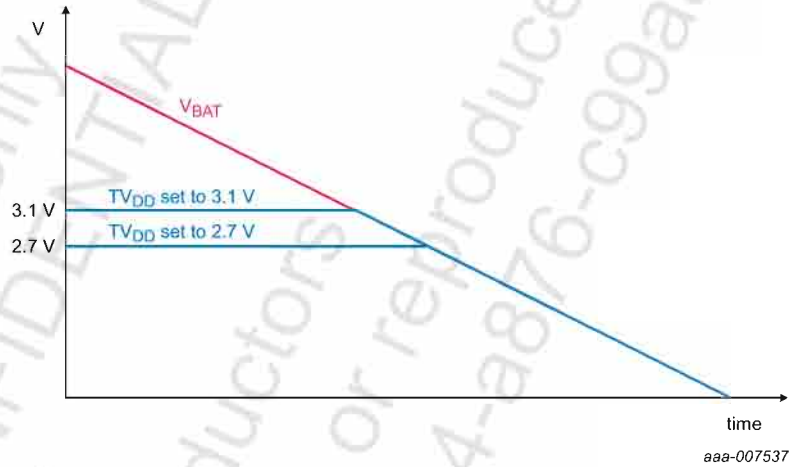


Fig 12. TV_{DD} offset disabled behavior

Figure 13 shows the case where the PN547/C2 is in Standby state:

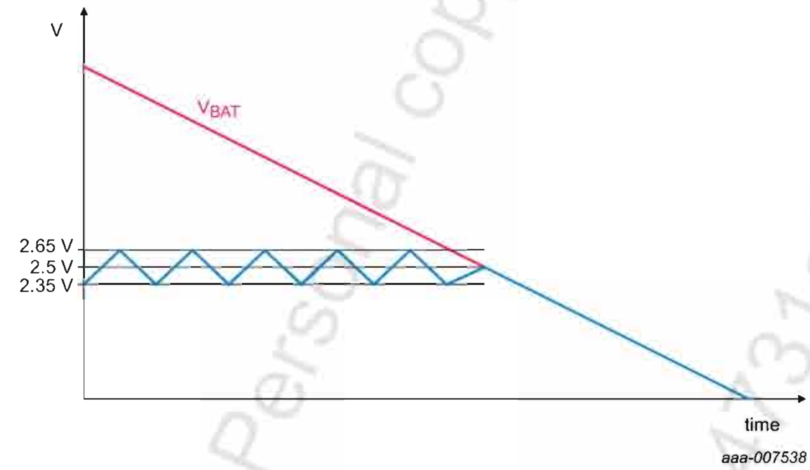


Fig 13. TV_{DD} behavior when PN547/C2 is in Standby state

10.6.3.1 TXLDO limiter

The TXLDO includes a current limiter to avoid too high current within TX1, TX2 when in Reader or Initiator states.

The current limiter block compares an image of the TXLDO output current to a reference. Once the reference is reached the output current gets limited which is equivalent to a typical output current of 220 mA for V_{BAT} = 2.7 V and 180 mA for V_{BAT} = 3.1 V.

10.6.4 Secure Element supply

A dedicated regulator is used to generate SV_{DD}.

This supply is used to supply a Secure Element connected on SWP.

References of SV_{DD} supply are in Table 1.

10.6.5 UICC supply

The UICC supply block is in charge to deliver the proper supply for the external UICC and also to provide SWIO data signal.

At the mobile device level, the UICC supply (UICC C1 pin = V_{CC} as described in the ETSI/SCP 102 221) might be connected to either PN547/C2 SIMVCC pin or directly to a PMU/LDO of the mobile device platform.

To allow the Card Emulation functionality when the mobile device is switched OFF then the UICC shall be powered via SIMVCC and PMUVCC shall be connected to the PMU/LDO output which is used as reference for the ETSI/SCP 102 221 interface of the UICC. $SIMV_{CC}$ voltage is present as soon as the PMU/LDO voltage is present and it is of the same class. PN547/C2 withstands 1.8 V (class C) or 3 V (class B).

The design is done such a way that SIMVCC can be low when the PN547/C2 is in Standby state. This is not the default configuration but it can be enabled by a firmware configuration (refer to Ref. 9).

When using PMU/LDO to directly supply the UICC, PMUVCC shall also be connected to the same supply in order to guarantee the compatibility of the SWIO S1 signal with the Ref. 1 specification for both 1.8 V (class C) or 3 V (class B). When in class C, the SWIO signal is directly generated from $PMUV_{CC}$ voltage, whereas in class B it is derived from DV_{DD}, internal 1.8 V reference.

When using SIMVCC to supply the UICC, then PMUVCC is connected to the PMU/LDO which gives the power supply used by the ETSI/SCP 102 221 interface. If the PMU/LDO is disabled, then a switch has been added to derive from DVDD, 1.8 V supply for SIMVCC, so that the PN547/C2 can still supply the UICC. As for DV_{DD}, $SIMV_{CC}$ is either generated from the remaining battery voltage. When PMUVCC supply is OFF, $SIMV_{CC}$ is only high when activity is required on SWIO.

In whatever mode the PN547/C2 is, including Hard Power Down (V_{EN} < 1.1 V), when $PMUV_{CC}$ rises, $SIMV_{CC}$ will follow $PMUV_{CC}$.

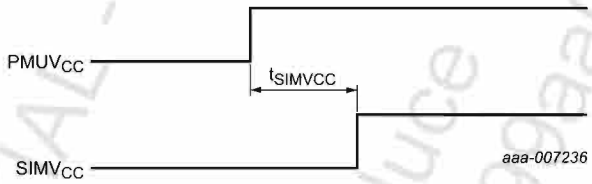


Fig 14. $SIMV_{CC}$ versus $PMUV_{CC}$

The PN547/C2 UICC circuitry is able to detect if $PMUV_{CC}$ is ON or OFF and from which class it is.

The On resistance of the internal switch between PMUVCC and SIMVCC is designed to be below 1 Ω in class B and below 1.2 Ω in class C. If this is too high for a given application, meaning that the voltage drop introduced by the switch is too high to keep the SIMVCC above the ETSI limits (that is, 2.7 V in class B and 1.62 V in class C), an external switch can be used to reduce the overall resistance of both switches in parallel. A signal is available on pin EXT_SW_CTRL to drive the gate of the external switch which has to be made of 2 transistors connected in series in order to cancel the parasitic diodes.

In case PMUVCC is present EXT_SW_CTRL pin is driven low otherwise it is driven high. In case SIMVCC is connected to PMUVCC, then EXT_SW_CTRL pin is driven low.

Remark: A possible reference is PMDPB65UP from NXP. The switch made with both transistors in series would have then the following max RdsOn: 210 mΩ × 2 = 420 mΩ at VGS = 1.8 V. assuming that the internal switch On resistance is 1500 mΩ, the overall On resistance would be ~330 mΩ.

10.6.6 Battery voltage monitor

The PN547/C2 features low-power V_{BAT} voltage monitor which protects mobile device battery from being discharged below critical levels. When V_{BAT} voltage goes below $V_{BATcritical}$ threshold then the PN547/C2 goes in monitor mode. Refer to Figure 15 for principle schematic of the battery monitor.

The battery voltage monitor is enabled via an EEPROM setting.

The $V_{BATcritical}$ threshold can be configured to 2.3 V or 2.75 V by an EEPROM setting.

At the first start-up, V_{BAT} voltage monitor functionality is OFF and then enabled if properly configured in EEPROM. The PN547/C2 monitors battery voltage continuously.

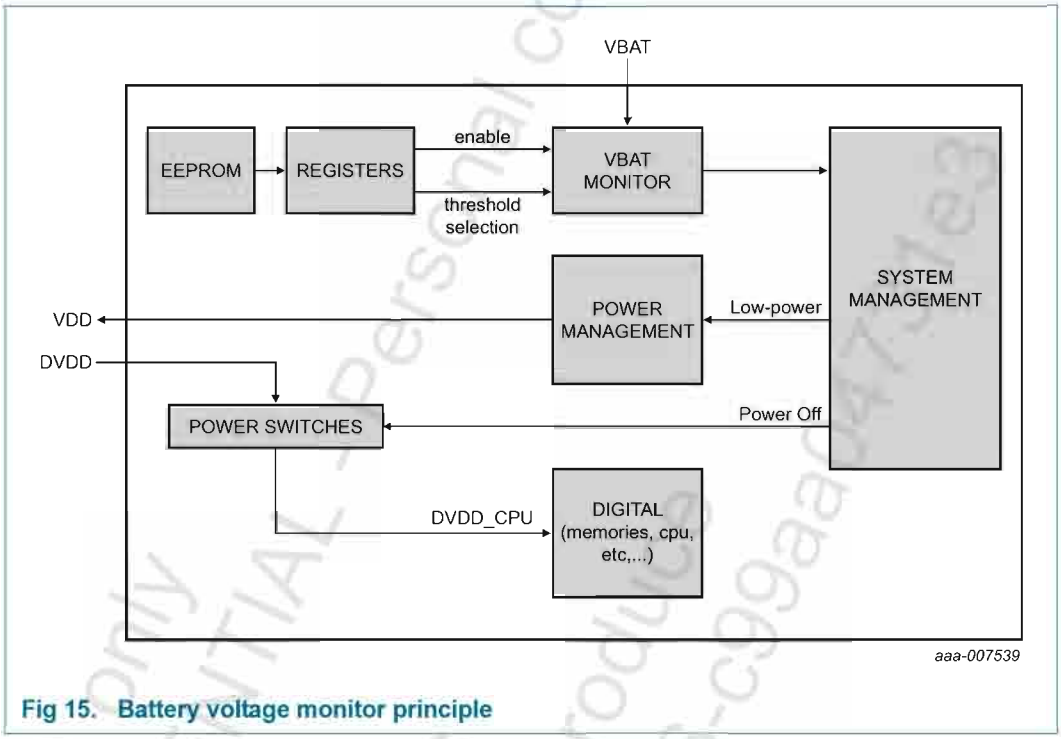


Fig 15. Battery voltage monitor principle

The value of the critical level can be configured to 2.3 V or 2.75 V by an EEPROM setting. This value has a typical hysteresis around 150 mV.

10.6.7 Thermal protection

In case of failure (short of TX1, TX2 or TVDD) the current consumption can increase up to the limiters value. The TXLDO can sink continuously up to around 180 mA for TV_{DD} = 3.1 V which are the thresholds of an internal limiter. Nevertheless the antenna shall be tuned so that the current within VBAT pin does not exceed 170 mA (see Table 1). The PN547/C2 will be heating, therefore a thermal protection is included.

The thermal protection is triggered at a threshold of 125 °C typical. In case over temperature is detected the embedded FW executes the following sequence:

- shuts down the TXLDO
- notifies host
- waits 50 ms to get host answer
- enters the Standby state, then no wake-up possible until over temperature disappears. In this mode, the PN547/C2 will consume around 100 µA as the temperature sensor remains active

After over temperature disappears the FW:

- wakes-up and goes to Active battery mode (ActiveBAT)
- notifies host

10.7 Contactless Interface Unit

PN547/C2 supports various communication modes at different transfer speeds and modulation schemes. The following chapters give more detailed overview of selected communication modes.

Remark: all indicated modulation index and modes in this chapter are system parameters. This means that beside the IC settings a suitable antenna tuning is required to achieve the optimum performance.

10.7.1 Reader/Writer modes

Generally 5 Reader/Writer modes are supported:

- PCD Reader/Writer for ISO/IEC 14443A/MIFARE
- PCD Reader/Writer for Jewel/Topaz tags
- PCD Reader/Writer for FeliCa cards
- PCD Reader/Writer for ISO/IEC 14443B
- VCD Reader/Writer for ISO/IEC 15693/ICODE

10.7.1.1 ISO/IEC 14443A/MIFARE and Jewel/Topaz PCD mode

The ISO/IEC 14443A/MIFARE PCD mode is the general reader to card communication scheme according to the ISO/IEC 14443A specification. This modulation scheme is as well used for communications with Jewel/Topaz cards.

Figure 16 describes the communication on a physical level, the communication table describes the physical parameters (the numbers take the antenna effect on modulation depth for higher data rates).

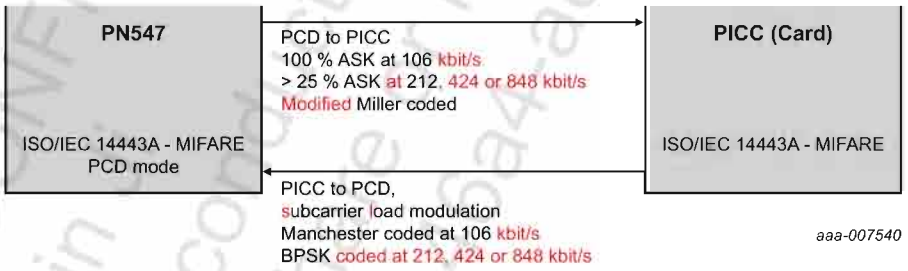


Fig 16. ISO/IEC 14443A/MIFARE Reader/Writer mode communication diagram

Table 20. Communication overview for ISO/IEC 14443A/MIFARE Reader/Writer

Communication direction		ISO/IEC 14443A/ MIFARE/Jewel/Topaz	ISO/IEC 14443A higher transfer speeds		
	Transfer speed	**106 kbit/s**	**212 kbit/s**	**424 kbit/s**	**848 kbit/s**
	Bit length	**(128/13.56) µs**	**(64/13.56) µs**	**(32/13.56) µs**	**(16/13.56) µs**
PN547/C2 → PICC					
(data sent by PN547/C2 to a card)	modulation on PN547/C2 side	100 % ASK	> 25 % ASK	> 25 % ASK	> 25 % ASK
	bit coding	Modified Miller	Modified Miller	Modified Miller	Modified Miller
PICC → PN547/C2					

Table 20. Communication overview for ISO/IEC 14443A/MIFARE Reader/Writer *...continued*

Communication direction		ISO/IEC 14443A/ MIFARE/Jewel/T opaz	ISO/IEC 14443A higher transfer speeds		
	Transfer speed	**106 kbit/s**	**212 kbit/s**	**424 kbit/s**	**848 kbit/s**
	Bit length	**(128/13.56) µs**	**(64/13.56) µs**	**(32/13.56) µs**	**(16/13.56) µs**
(data received by PN547/C2 from a card)	modulation on PICC side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	bit coding	Manchester	BPSK	BPSK	BPSK

The contactless coprocessor and the on-chip CPU of PN547/C2 handle the complete ISO/IEC 14443A/MIFARE RF-protocol, nevertheless a dedicated external host has to handle the application layer communication.

10.7.1.2 FeliCa PCD mode

The FeliCa mode is the general Reader/Writer to card communication scheme according to the FeliCa specification. Figure 17 describes the communication on a physical level, the communication overview describes the physical parameters.

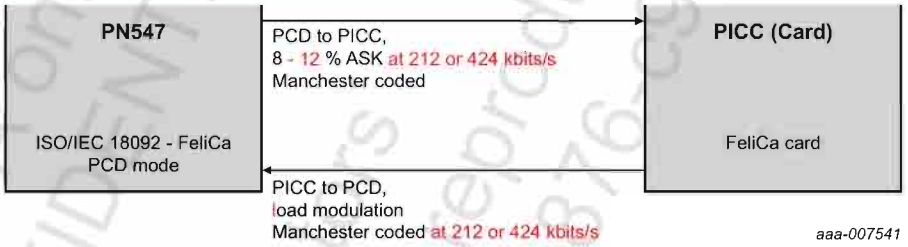


Fig 17. FeliCa Reader/Writer communication diagram

Table 21. Communication overview for FeliCa Reader/Writer

Communication direction		FeliCa	FeliCa higher transfer speeds
	Transfer speed	**212 kbit/s**	**424 kbit/s**
	Bit length	**(64/13.56) µs**	**(32/13.56) µs**
PN547/C2 → PICC			
(data sent by PN547/C2 to a card)	modulation on PN547/C2 side	8 % – 12 % ASK	8 % – 12 % ASK
	bit coding	Manchester	Manchester
PICC → PN547/C2			
(data received by PN547/C2 from a card)	modulation on PICC side	load modulation	load modulation
	subcarrier frequency	no subcarrier	no subcarrier
	bit coding	Manchester	Manchester

The contactless coprocessor of PN547/C2 and the on-chip CPU handle the FeliCa protocol. Nevertheless a dedicated external host has to handle the application layer communication.

10.7.1.3 ISO/IEC 14443B PCD mode

The ISO/IEC 14443-B PCD mode is the general reader to card communication scheme according to the ISO/IEC 14443-B specification.Figure 18 describes the communication on a physical level, the communication table describes the physical parameters.

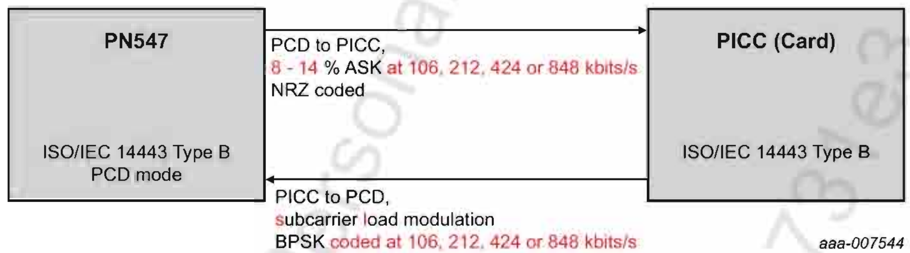


Fig 18. ISO/IEC 14443B reader/writer communication diagram

Table 22. Communication overview for ISO/IEC 14443B Reader/Writer

Communication direction		ISO/IEC 14443B	ISO/IEC 14443B higher transfer speeds		
	Transfer speed	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
	Bit length	(128/13.56) µs	(64/13.56) µs	(32/13.56) µs	(16/13.56) µs
PN547/C2 → PICC					
(data sent by PN547/C2 to a card)	modulation on PN547/C2 side	8 % – 14 % ASK	8 % – 14 % ASK	8 % – 14 % ASK	8 % – 14 % ASK
	bit coding	NRZ	NRZ	NRZ	NRZ
PICC → PN547/C2					
(data received by PN547/C2 from a card)	modulation on PICC side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	bit coding	BPSK	BPSK	BPSK	BPSK

The contactless coprocessor and the on-chip CPU of PN547/C2 handles the complete ISO/IEC 14443-B RF-protocol, nevertheless a dedicated external host has to handle the application layer communication.

10.7.1.4 ISO/IEC 15693 VCD mode

The ISO/IEC 15693 VCD Reader/Writer mode is the general reader to card communication scheme according to the ISO/IEC 15693 specification. PN547/C2 will communicate with VICC using only the higher data rates of the VICC (26.48 kbit/s with single subcarrier and 26.69 kbit/s with dual subcarrier).

PN547/C2 supports the commands as defined by the ETSI HCI (see Ref. 2), and on top offers the inventory of the tags (anticollision sequence) on its own.

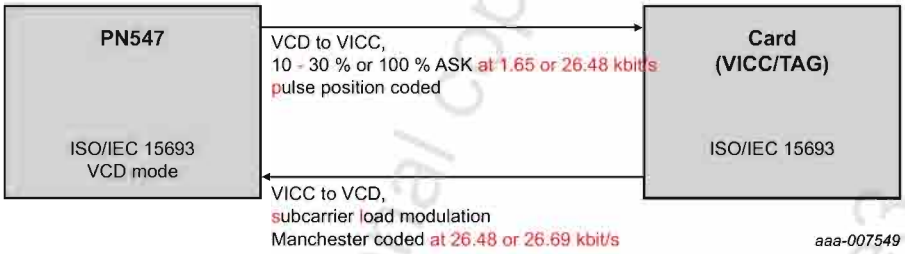


Fig 19. ISO/IEC 15693 VCD mode communication diagram

Figure 19 shows the communication schemes used.

2 communication schemes can be used from card to PN547/C2 and 2 communication schemes can be used from PN547/C2 to card.

Thus, 4 communication schemes are possible.

Table 23. Communication overview for ISO/IEC 15693 VCD

Communication direction			
PN547/C2 → VICC			
(data sent by PN547/C2 to a tag)	transfer speed	1.65 kbit/s	26.48 kbit/s
	bit length	(8192/13.56) µs	(512/13.56) µs
	modulation on PN547/C2 side	10 % – 30 % or 100 % ASK	10 % – 30 % or 100 % ASK
	bit coding	pulse position modulation 1 out of 256 mode	pulse position modulation 1 out of 4 mode
VICC → PN547/C2			
(data received by PN547/C2 from a tag)	transfer speed	26.48 kbit/s	26.69 kbit/s
	bit length	(512/13.56) µs	(508/13.56) µs
	modulation on VICC side	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	single subcarrier	dual subcarrier
	bit coding	Manchester	Manchester

10.7.2 ISO/IEC 18092, Ecma 340 NFCIP-1 operating mode

An NFCIP-1 communication takes place between 2 devices:

- Initiator: generates RF field at 13.56 MHz and starts the NFCIP-1 communication
- Target: responds to Initiator command either in a load modulation scheme in Passive Communication mode or using a self generated and self modulated RF field for Active Communication mode

The NFCIP-1 communication differentiates between Active and Passive Communication modes.

- Active Communication mode means both the Initiator and the Target are using their own RF field to transmit data
- Passive Communication mode means that the Target answers to an Initiator command in a load modulation scheme. The Initiator is active in terms of generating the RF field

In order to fully support the NFCIP-1 standard PN547/C2 supports the Active and Passive Communications mode at the transfer speeds 106 kbit/s, 212 kbit/s and 424 kbit/s as defined in the NFCIP-1 standard.

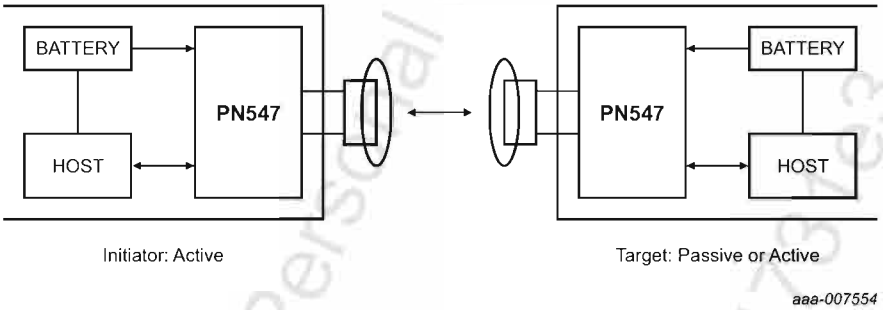


Fig 20. NFCIP-1 mode

The contactless coprocessor of PN547/C2 and the on-chip CPU handle NFCIP-1 protocol, for all communication modes and data rates, for both Initiator and Target.

Nevertheless a dedicated external host has to handle the application layer communication.

10.7.2.1 Passive Communication mode

Passive Communication mode means that the Target answers to an Initiator command in a load modulation scheme.

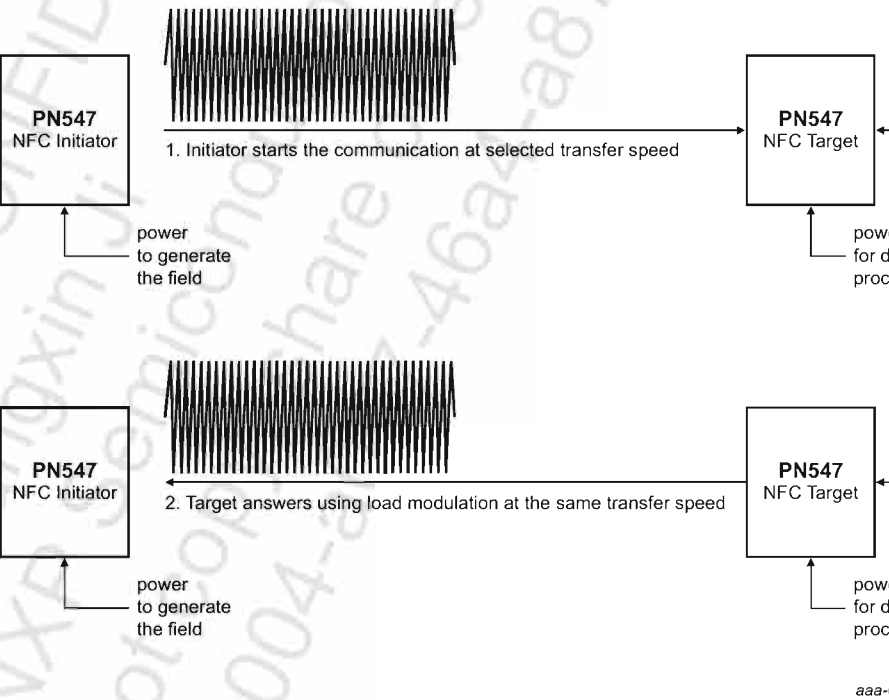


Fig 21. Passive NFC mode

Table 24 gives an overview of the Passive NFC mode:

Table 24. Communication overview for Passive NFC mode

Communication direction		ISO/IEC 18092, Ecma 340, NFCIP-1		
	Baud rate	106 kbit/s	212 kbit/s	424 kbit/s
	Bit length	(128/13.56) µs	(64/13.56) µs	(32/13.56) µs
Initiator to Target				
	modulation	100 % ASK	8 % – 30 % ASK[1]	8 % – 30 % ASK[1]
	bit coding	Modified Miller	Manchester	Manchester
Target to Initiator				
	modulation	subcarrier load modulation	load modulation	load modulation
	subcarrier frequency	13.56 MHz/16	no subcarrier	no subcarrier
	bit coding	Manchester	Manchester	Manchester

[1] This modulation index range is according NFCIP-1 standard. It might be that some NFC forum type 3 cards does not withstand the full range as based on FeliCa range which is narrow (8 % to 14 % ASK). To adjust the index look to Ref. 11.

10.7.2.2 NFCIP-1 framing and coding

The NFCIP-1 framing and coding in Active and Passive Communication modes are defined in the NFCIP-1 standard: ISO/IEC 18092 or Ecma 340.

10.7.2.3 NFCIP-1 protocol support

The NFCIP-1 protocol is not completely described in this document. For detailed explanation of the protocol, refer to the ISO/IEC 18092 or Ecma 340 NFCIP-1 standard. However the datalink layer is according to the following policy:

- Transaction includes initialization, anticollision methods and data transfer. This sequence must not be interrupted by another transaction
- PSL shall be used to change the speed between the target selection and the data transfer, but the speed should not be changed during a data transfer

10.7.3 Card operation modes

PN547/C2 can be addressed as a ISO/IEC 14443A, MIFARE, ISO/IEC 14443B cards. This means that PN547/C2 can generate an answer in a load modulation scheme according to the ISO/IEC 14443A, ISO/IEC 14443B interface description.

MIFARE is supported via SWP CLT.

FeliCa is supported via SWP CLT.

Remark: PN547/C2 does not support a complete card protocol. This has to be handled either by a connected companion Secure Element or the host controller.

Table 25 and Table 26 describe the physical parameters.

10.7.3.1 ISO/IEC 14443A/MIFARE card operation mode

Table 25. Communication overview for ISO/IEC 14443A/MIFARE card operation mode

Communication direction		ISO/IEC 14443A/MIFARE	ISO/IEC 14443A higher transfer speeds	
	Transfer speed	106 kbit/s	212 kbit/s	424 kbit/s
	Bit length	(128/13.56) µs	(64/13.56) µs	(32/13.56) µs
PCD → PN547/C2				
(data received by PN547/C2 from a card)	modulation on PCD side	100 % ASK	> 25 % ASK	> 25 % ASK
	bit coding	Modified Miller	Modified Miller	Modified Miller
PN547/C2 → PCD				
(data sent by PN547/C2 to a card)	modulation on PN547/C2 side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	bit coding	Manchester	BPSK	BPSK

10.7.3.2 ISO/IEC 14443B card operation mode

Table 26. Communication overview for ISO/IEC 14443B card operation mode

Communication direction		ISO/IEC 14443B	ISO/IEC 14443B higher transfer speeds	
	Transfer speed	106 kbit/s	212 kbit/s	424 kbit/s
	Bit length	(128/13.56) µs	(64/13.56) µs	(32/13.56) µs
PCD → PN547/C2				
(data received by PN547/C2 from a Reader)	modulation on PCD side	8 % – 14 % ASK	8 % – 14 % ASK	8 % – 14 % ASK
	bit coding	NRZ	NRZ	NRZ
PN547/C2 → PCD				
(data sent by PN547/C2 to a Reader)	modulation on PN547/C2 side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	bit coding	BPSK	BPSK	BPSK

10.7.4 Frequency interoperability

When in communication, PN547/C2 is generating some RF frequencies. PN547/C2 is also sensitive to some RF signals as it is looking from data in the field.

In order to avoid interference with others RF communication it is required to tune the antenna and design the board according to Ref. 10.

Although ISO/IEC 14443 and ISO/IEC 18092/Ecma 340 allows an RF frequency of 13.56 MHz ± 7 kHz, FCC regulation does not allow this wide spread and limits the dispersion to ± 50 ppm, which is in line with PN547/C2 capability.

10.8 Support for production test and implementation

PN547/C2 supports several tests functions which ease test in final application production environment.

- Antenna self test:

  If the antenna tuning is done according to recommendations given in Ref. 11, this test can detect that all tuning components are present with the right value. This process requires a calibration process.

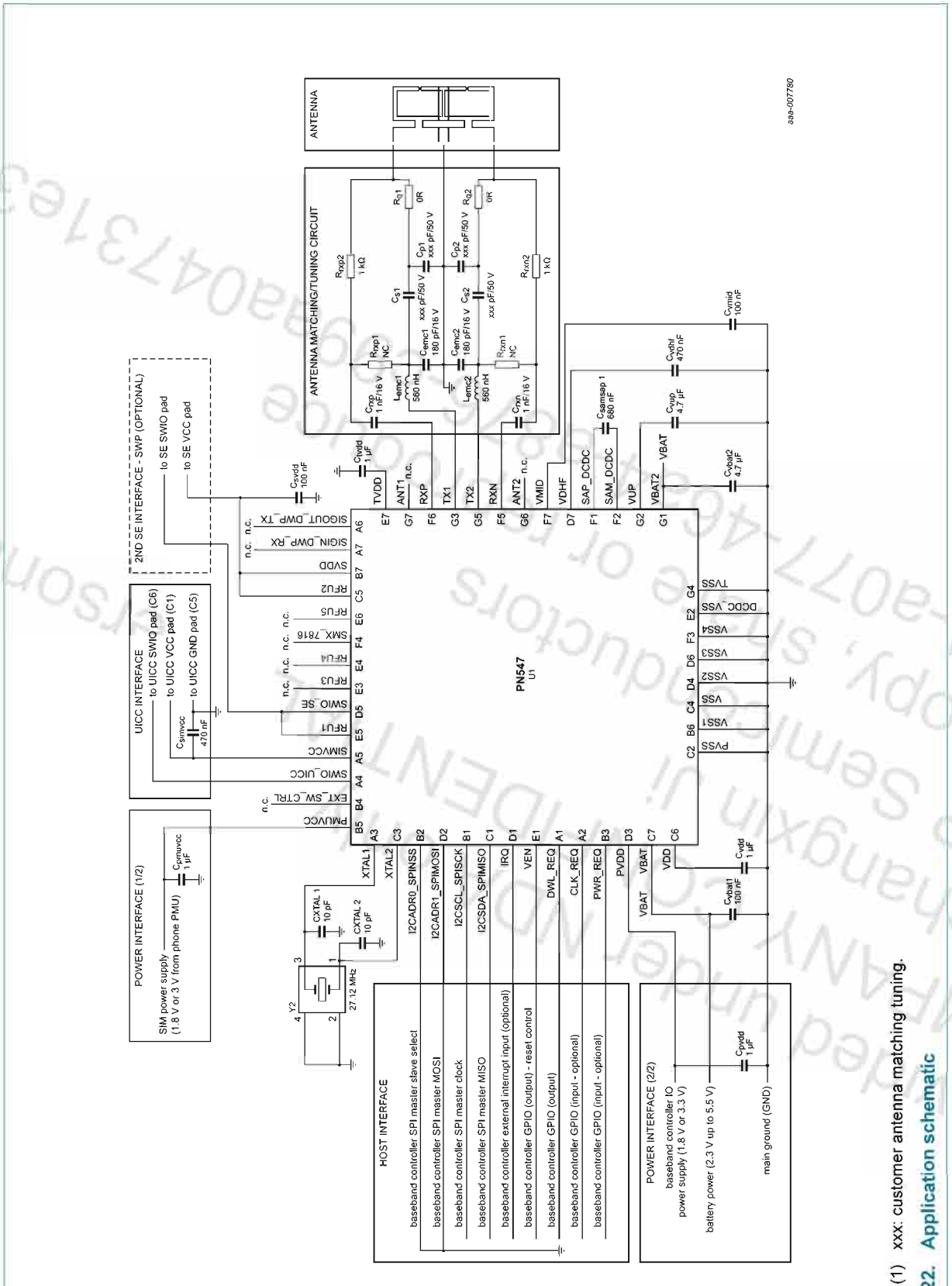
  Refer to Ref. 9 to know how to use the associated commands.

- SWP self test:

  This function checks the connection of SWIO and PMUVCC lines.

  Refer to Ref. 9 to know how to use the associated commands.

11. Application design-in information



(1) xxx: customer antenna matching tuning.

Fig 22. Application schematic

12. Limiting values

Table 27. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
PV_{DD}	pad supply voltage		-	3.6	V
V_{BAT}	power supply voltage		-	6	V
$V_{BATDCDC}$	power supply voltage		-	6	V
V_{ESDH}	ESD susceptibility (Human Body Model)	1500 Ω, 100 pF; EIA/JESD22-A114-D	-	1.5	kV
V_{ESDC}	ESD susceptibility (Charge Device Model)	field induced model; EIA/JESC22-C101-C	-	500	V
T_{stg}	storage temperature		–55	+150	°C
P_{tot}	total power dissipation	all modes [1]	-	0.55	W

[1] The design of the solution shall be done so that for the different use cases targeted the power to be dissipated from the field or generated by PN547/C2 does not exceed this value.

13. Recommended operating conditions

Table 28. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb}	operating ambient temperature	JEDEC PCB-0.5	–30	+25	+85	°C
V_{BAT}	battery supply voltage	battery monitor enabled V_{SS} = 0 V	2.3	-	5.5	V
V_{BAT}	power supply voltage	Card Emulation and Passive Target V_{SS} = 0 V [1][2]	2.3	-	5.5	V
V_{BAT}	power supply voltage	Reader, Active Initiator and Active Target V_{SS} = 0 V [1][2]	2.7	-	5.5	V
PV_{DD}	supply voltage for host interface	1.8 V host supply V_{SS} = 0 V [1]	1.65	1.8	1.95	V
PV_{DD}	supply voltage for host interface	3 V host supply V_{SS} = 0 V [1]	2.7	3.0	3.3	V
P_{tot}	total power dissipation	Reader I_{TVDD} = 100 mA V_{BAT} = 5.5 V	-	-	0.5	W
I_{TVDD}	maximum current in TVDD	[2]	100	-	-	mA
I_{SVDD}	maximum current in SVDD switch	V_{BAT} > 2.3 V	20	-	-	mA

[1] V_{SS} represents PV_{SS}, DV_{SS}, TV_{SS1}, TV_{SS2}.

[2] The antenna should be tuned not to exceed this current limit (the detuning effect when coupling with another device must be taken into account).

14. Thermal characteristics

Table 29. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{thj-a}	thermal resistance from junction to ambient	in free air with exposed pad soldered on a 4 layer JEDEC PCB	-	<tbd>	-	K/W

15. Characteristics

15.1 Current consumption characteristics

Table 30. Current consumption characteristics for operating ambient temperature range

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{HPD}	Hard Power Down current on VBAT	V_{BAT} = 3.6 V; V_{EN} = 0 V		-	10	18	µA
I_{STBY}	Standby state current on VBAT (including emulation phase of polling loop)	V_{BAT} = 3.6 V	[1]	-	20	35	µA
I_{ACT}	Active state current on VBAT in Idle and Target power modes	V_{BAT} = 3.6 V	[2]	-	6	-	mA
I_{RFON}	Active state current on VBAT in Initiator power mode	V_{BAT} = 3 .6 V	[2]	-	13	-	mA
I_{MON}	monitor mode current on VBAT	V_{BAT} = 2.75 V	[3]	-	10	18	µA
I_{TVDD}	transmitter supply current	continuous wave, TV_{DD} = 3.1 V	[4][5]	-	30	100	mA
I_{PMUVCC}	PMUVCC supply current consumes by PN547/C2 VFBGA in Standby and HPD states	class B		-	1.5	3	µA
		class C		-	1	2	µA

[1] Refer to Section 10.1.2.4 for the description of the power modes.

[2] Refer to Section 10.1.2.5 for the description of the polling loop.

[3] This is the same value for V_{BAT} = 2.3 V when the monitor threshold is set to 2.3 V.

[4] I_{TVDD} depends on TV_{DD} and on the external circuitry connected to Tx1 and Tx2.

[5] During operation with a typical circuitry as recommended by NXP in Ref. 11, the overall current is below 100 mA even when loaded by target/card/tag.

15.2 Functional block electrical characteristics

15.2.1 Battery voltage monitor characteristics

Table 31. Battery voltage monitor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{THRES}	threshold voltage	set to 2.3 V	2.2	2.3	2.4	V
V_{THRES}	threshold voltage	set to 2.75 V	2.65	2.75	2.85	V
V_{HYST}	hysteresis voltage		100	150	200	mV

15.2.2 Reset via VEN

Table 32. Reset timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RESETVEN}$	VEN pulse width to reset		3	-	-	µs
t_{BOOT}	boot time		-	-	2.5	ms

15.2.3 Power-up timings

Table 33. Power-up timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{VBATVEN}$	minimum time from V_{BAT} high to V_{EN} high		0	-	-	ms
$t_{PVDDVEN}$	minimum time from PV_{DD} high to V_{EN} high		0	-	-	ms

15.2.4 Download mode timings

Table 34. Download mode timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{GPIO4VEN}$	minimum time from DWL_REQ voltage high to V_{EN} high		0	-	-	ms

15.2.5 Thermal protection

Table 35. Thermal threshold

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{overtemp}$	high temperature at which the thermal protection is triggered		120	125	130	°C

15.2.6 I²C-bus timings

Here below are timings and frequency specifications.

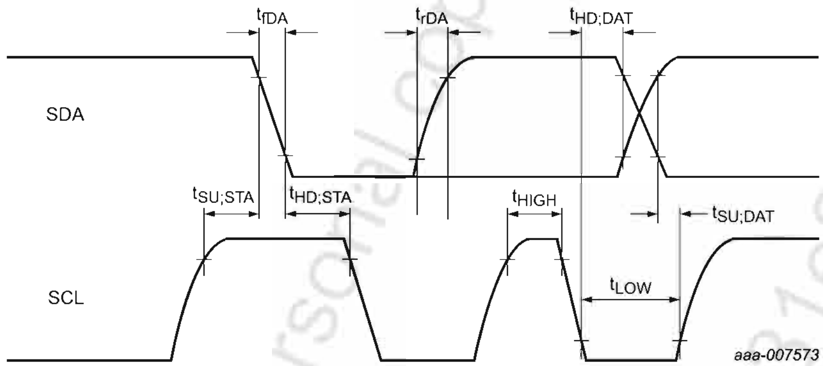


Fig 23. I²C-bus timings

Table 36. High-speed mode I²C-bus timings specification

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCLH}	SCLH clock frequency	C_b < 100 pF	0	3.4	MHz
$t_{SU;STA}$	set-up time for a (repeated) START condition	C_b < 100 pF	160	-	ns
$t_{HD;STA}$	hold time (repeated) START condition	C_b < 100 pF	160	-	ns
t_{LOW}	LOW period of the SCL clock	C_b < 100 pF	160	-	ns
t_{HIGH}	HIGH period of the SCL clock	C_b < 100 pF	60	-	ns
$t_{SU;DAT}$	data set-up time	C_b < 100 pF	10	-	ns
$t_{HD;DAT}$	data hold time	C_b < 100 pF	0	-	ns
t_{rDA}	rise time of SDA	C_b < 100 pF	10	80	ns
t_{fDA}	fall time of SDA	C_b < 100 pF	10	80	ns
V_{hys}	hysteresis of Schmitt trigger inputs	C_b < 100 pF	$0.1PV_{DD}$	-	V

Table 37. Fast mode I²C-bus timings specification

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCLH}	SCLH clock frequency	C_b < 400 pF	0	400	kHz
$t_{SU;STA}$	set-up time for a (repeated) START condition	C_b < 400 pF	600	-	ns
$t_{HD;STA}$	hold time (repeated) START condition	C_b < 400 pF	600	-	ns
t_{LOW}	LOW period of the SCL clock	C_b < 400 pF	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock	C_b < 400 pF	600	-	ns
$t_{SU;DAT}$	data set-up time	C_b < 400 pF	100	-	ns
$t_{HD;DAT}$	data hold time	C_b < 400 pF	0	900	ns
V_{hys}	hysteresis of Schmitt trigger inputs	C_b < 400 pF	$0.1PV_{DD}$	-	V

15.2.7 SPI-bus timings

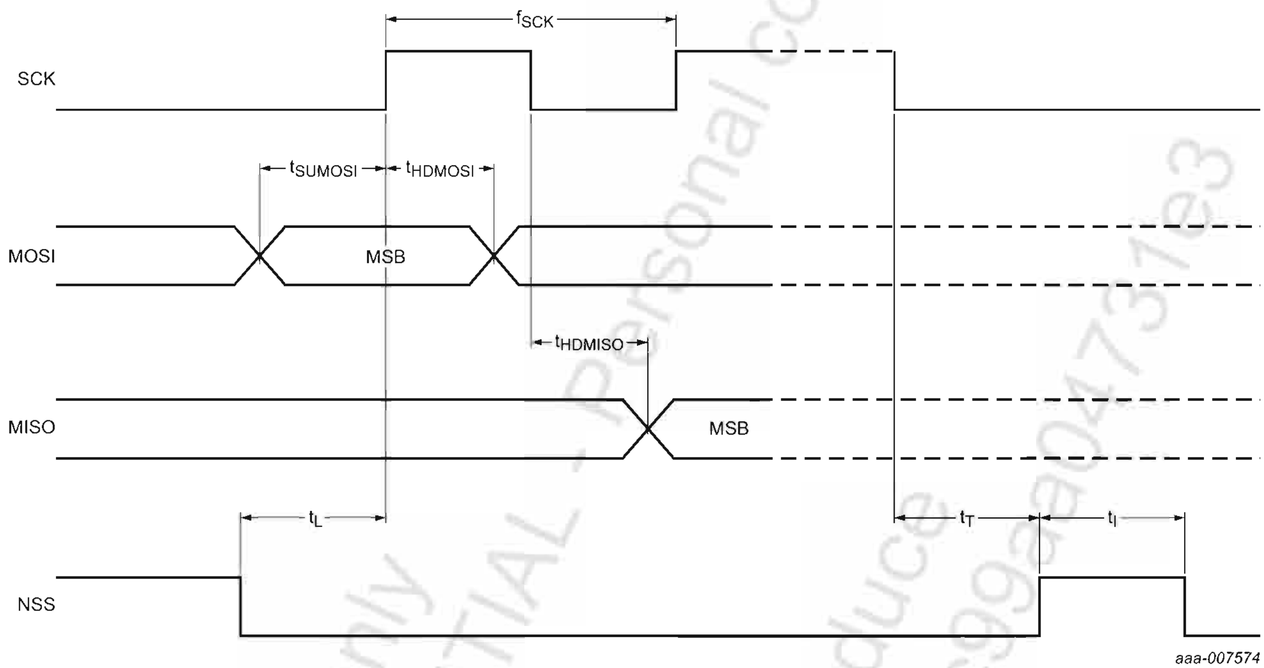


Fig 24. SPI-bus timing diagram

Table 38. SPI-bus timings specification

Symbol	Parameter	Conditions	Min	Max	Unit
t_{SCK}	clock period of SCK		-	142	ns
t_{SUMOSI}	set-up time of the MOSI line before the sampling edge of SCK	[1]	35	-	ns
t_{HDMOSI}	hold time of the MOSI line after the sampling edge of SCK	[1]	35	-	ns
t_{HDMISO}	hold time of the MOSI line before the changing edge of SCK	[2]	-	35	ns
t_{HDnss}	hold time of the NSS line changing to high after the last changing edge of SCK	[1]	35	-	ns
t_{SUnss}	set-up time of the NSS line changing to low before the first change of SCK	[1]	142	-	ns

[1] Controlled by host.

[2] Controlled by PN547/C2.

15.2.8 UICC supply characteristics

See Table 39 for the parameters of the UICC supply functionality.

Table 39. Electrical characteristics of UICC supply

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$PMUV_{CC\_Thresh}$	threshold for $PMUV_{CC}$ at which $SIMV_{CC}$ is supplied from $PMUV_{CC}$		0.7	-	1.1	V
ClassB_thresh	Class B detection threshold for $PMUV_{CC}$		2.1	2.4	2.6	V
$SIMV_{CC}$	SIMVCC voltage	$PMUV_{CC}$ to ground I_{SIMVCC} = 5 mA	1.62	-	1.98	V
Ron_B	resistance between PMUVCC and SIMVCC	$PMUV_{CC}$ = 2.75 V, I_{SIMVCC} = 50 mA	-	-	1.0	Ω
Ron_C	resistance between PMUVCC and SIMVCC	$PMUV_{CC}$ = 1.67 V I_{SIMVCC} = 30 mA	-	-	1.2	Ω
Ron_PD	resistance between SIMVCC and VSS when UICC is not powered	DV_{DD} = 1.65 V	-	-	0.4	kΩ

15.3 Pin characteristics

15.3.1 XTAL pin characteristics (XTAL1, XTAL2)

Table 40. Input clock characteristics on XTAL1 when using PLL

Parameter	Conditions	Min	Typ	Max	Unit
peak-to-peak input voltage		0.2	-	1.65	V
duty cycle		35	-	65	%

Table 41. Pin characteristics for XTAL1 when PLL input

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IH}	HIGH-level input current	$V_I = V_{DD}$	-	-	1	µA
I_{IL}	LOW-level input current	V_I = 0 V	−1	-	-	µA
V_I	input voltage		-	-	V_{DD}	V
V_{AL}	input voltage amplitude		200	-	-	mV
C_{IN}	input capacitance	all power modes	-	2	-	pF

Table 42. Pin characteristics for 27.12 MHz crystal oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{INXTAL1}$	XTAL1 input capacitance	V_{DD} = 1.8 V, V_{DC} = 0.65 V, V_{AC} = 0.9 V(p-p) [1]	-	2	-	pF
$C_{INXTAL2}$	XTAL2 input capacitance		-	2	-	pF

[1] See the Figure 22 for example of appropriate connected components. The layout should ensure minimum distance between the pins and the components.

Table 43. PLL accuracy

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{acc}	deviation added to XTAL1 frequency on RF frequency generated	worst case whatever input frequency	−50	-	+50	ppm

15.3.2 VEN input pin characteristics

Table 44. VEN input pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		1.1	-	V_{BAT}	V
V_{IL}	LOW-level input voltage		0	-	0.4	V
I_{IH}	HIGH-level input current	$V_{EN} = V_{BAT}$	-	-	1	μA
I_{IL}	LOW-level input current	$V_{EN} = 0$ V	−1	-	-	μA
C_{IN}	input capacitance		-	5	-	pF

15.3.3 Output pin characteristics for IRQ, CLK_REQ and PWR_REQ

Table 45. Output pin characteristics for IRQ, CLK_REQ and PWR_REQ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$I_{OH} < 3$ mA	$PV_{DD} - 0.4$	-	PV_{DD}	V
V_{OL}	LOW-level output voltage	$I_{OL} < 3$ mA	0	-	0.4	V
C_L	load capacitance		-	-	20	pF
t_{fall}	fall times	$C_L = 12$ pF max				
		high speed	1	-	3	ns
		slow speed	3	-	10	ns
t_{rise}	rise times	$C_L = 12$ pF max				
		high speed	1	-	3	ns
		slow speed	3	-	10	ns
	extra pull-down	[1]	0.4	-	0.75	MΩ

[1] Extra pull-down is activated in HPD state and monitor mode.

15.3.4 Output pin characteristics for DWL_REQ

Table 46. Output pin characteristics for DWL_REQ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	$PV_{DD} = 1.8$ V	$0.65PV_{DD}$		-	V
V_{IL}	LOW-level output voltage	$PV_{DD} = 1.8$ V	-	-	$0.35PV_{DD}$	V
V_{IH}	HIGH-level input voltage	$PV_{DD} = 3$ V	2	-	-	V
V_{IL}	LOW-level output voltage	$PV_{DD} = 3$ V	-	-	0.8	V
I_{IH}	HIGH-level input current		-	-	1	mA

Table 46. Output pin characteristics for DWL_REQ *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IL}	LOW-level input current		−1	-	-	mA
C_{IN}	input capacitance		-	-	5	pF
	extra pull-down	[1]	0.4	-	0.75	MΩ

[1] Extra pull-down is activated in HPD state and monitor mode.

15.3.5 Output pin characteristics for I2CADR0_SPINSS, I2CADR1_SPIMOSI, I2CSCL_SPISCK (used as SPISCK)

Table 47. Output pin characteristics for I2CADR0_SPINSS, I2CADR1_SPIMOSI, I2CSCL_SPISCK (used as SPISCK)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		$0.65PV_{DD}$	-	PV_{DD}	V
V_{IL}	LOW-level input voltage		0	-	$0.35PV_{DD}$	V
I_{IH}	HIGH-level input current	$V_I = PV_{DD}$; T = 125 °C	-	-	1	µA
I_{IL}	LOW-level input current	$V_I = 0$ V; T = 125 °C	−1	-	-	µA
C_{IN}	input capacitance		-	5	-	pF

15.3.6 Pin characteristics for I2CSDA_SPIMISO (used as I2CSDA) and I2CSCL_SPISCK (used as I2CSCL)

Table 48. Pin characteristics I2CSDA_SPIMISO (used as I2CSDA) and I2CSCL_SPISCK (used as I2CSCL)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$I_{OL} < 3$ mA	0	-	0.4	V
C_L	load capacitance		-	-	10	pF
t_{fall}	fall times	$C_L = 100$ pF, Rpull-up = 2 kΩ Standard and Fast mode	30	-	250	ns
t_{fall}	fall times	$C_L = 100$ pF, Rpull-up = 1 kΩ High-speed mode	110	-	80	ns
t_{rise}	rise times	$C_L = 100$ pF, Rpull-up = 2 kΩ Standard and Fast mode	30	-	250	ns
t_{rise}	rise times	$C_L = 100$ pF, Rpull-up = 1 kΩ High-speed mode	10	-	100	ns
V_{IH}	HIGH-level input voltage		$0.7PV_{DD}$	-	PV_{DD}	V
V_{IL}	LOW-level input voltage		0	-	$0.3PV_{DD}$	V
I_{IH}	HIGH-level input current	$V_I = PV_{DD}$; high impedance	-	-	1	µA
I_{IL}	LOW-level input current	$V_I = 0$ V; high impedance	−1	-	-	µA
C_{IN}	input capacitance		-	5	-	pF

15.3.7 Pin characteristics for I2CSDA_SPIMISO

Table 49. Pin characteristics I2CSDA_SPIMISO

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} < 4 mA	PV_{DD} – 0.4	-	PV_{DD}	V
V_{OL}	LOW-level output voltage	I_{OL} < 4 mA	0	-	0.4	V
C_L	load capacitance		-	-	20	pF
t_{fall}	fall times	C_L = 12 pF max				
		high speed	1	-	3	ns
		slow speed	3	-	10	ns
t_{rise}	rise times	C_L = 12 pF max				
		high speed	1	-	3	ns
		slow speed	3	-	10	ns

15.3.8 SWIO_UICC pin characteristics

Table 50. Electrical characteristics of SWIO_UICC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SWIO_VOH_B	output high voltage; $PMUV_{CC}$ in class B	I_{SWIO_UICC} = 1 mA I_{SIMVCC} = 50 mA $PMUV_{CC}$ = 2.75 V	[1]	1.4	-	-	V
SWIO_VOH_C_ext	output high voltage; $PMUV_{CC}$ in class C	I_{SWIO_UICC} = 1 mA I_{SIMVCC} = 30 mA $PMUV_{CC}$ = 1.67 V	[1]	0.85$SIMV_{CC}$	-	-	V
SWIO_VOH_C_int	output high voltage; $SIMV_{CC} = DV_{DD}$	I_{SWIO_UICC} = 1 mA I_{SIMVCC} = 5 mA $PMUV_{CC}$ = 0 V	[1]	0.85$SIMV_{CC}$	-	-	V
SWIO_VOL	output low voltage	0 µA < I_{SWIO_UICC} < 20 µA	[1]	-	-	0.3	V
SWIO_IIH	current threshold			180	300	420	µA
I_{leak}	leakage current	high impedance		–1	-	+1	µA

[1] To allow for overshoot the voltage on SWIO shall remain between –0.3 V and $V_{OH\ max}$ + 0.3 V during dynamic operation.

15.3.9 Output pin characteristics for EXT_SW_CTRL

Table 51. Output pin characteristics for EXT_SW_CTRL

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} < 100 µA	DV_{dd} – 0.1	-	D_{dd}	V
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA	0	-	0.1	V
$t_{rise,fall}$	rise and fall times	C_L = 1 nF	-	10	-	µs
C_{OUT}	output capacitance		-	-	2	nF

15.3.10 SWIO_SE pin characteristics

Table 52. Electrical characteristics of SWIO_SE

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SWIO_VOH	output high voltage	I_{SWIO_SE} = 1 mA	[1]	$0.85SV_{DD}$	-	-	V
SWIO_VOL	output low voltage	0 µA < I_{SWIO_SE} < 20 µA	[1]	-	-	0.3	V
SWIO_IIH	current threshold			180	300	420	µA
I_{leak}	leakage current	high impedance		−1	-	+1	µA

[1] To allow for overshoot the voltage on SWIO shall remain between −0.3 V and $V_{OH\ max}$ + 0.3 V during dynamic operation

15.3.11 ANT1 and ANT2 pin characteristics

Table 53. Electrical characteristics of ANT1 and ANT2

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{ON}	impedance between ANT1 and ANT2	low impedance	-	10	17	Ω
V_{LIM}	limiter threshold on ANT1 and ANT2	I = 10 mA	-	3.3	-	V

15.3.12 Input pin characteristics for RXN and RXP

Table 54. Input pin characteristics for RXN and RXP

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{INRX}	dynamic input voltage range		[1]	0	-	V_{DD}	V
C_{INRX}	RXN and RXP input capacitance			-	12	-	pF
R_{RXVMID}	impedance from RX to VMID	Reader, Card and P2P modes		0	-	15	kΩ
$V_{RX,MinIV,Mill}$	minimum dynamic input voltage, Miller coded	106 kbit/s		-	150	200	mV(p-p)
		212 kbit/s to 424 kbit/s		-	150	200	mV(p-p)
$V_{RX,MinIV,Man}$	minimum dynamic input voltage, Manchester, NRZ or BPSK coded	106 kbit/s to 848 kbit/s		-	150	200	mV(p-p)
$V_{RX,MaxIV,Mill}$	maximum dynamic input voltage, all data coding	106 kbit/s to 848 kbit/s	[1]	V_{DD}	-	-	V(p-p)
$V_{RFdetect}$	RF input voltage detected	Initiator modes		-	100	-	mV(p-p)

[1] It is therefore recommended to design the application so that RXN and RXP voltage never exceeds $V_{DD(min)}$ = 1.65 V.

15.3.13 Output pin characteristics for TX1 and TX2

Table 55. Output pin characteristics for TX1 and TX2

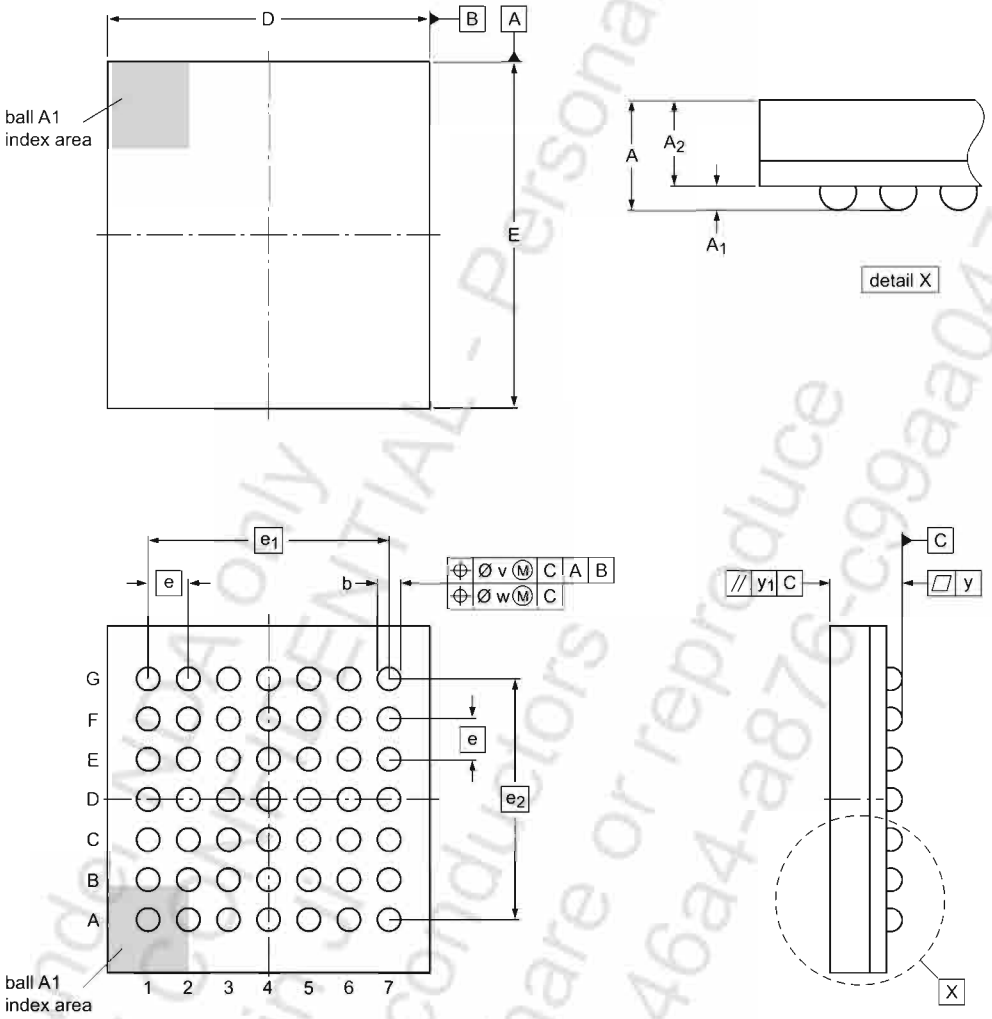
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OH,\ C32,\ 3\ V}$	HIGH-level output voltage	TV_{DD} = 3.1 V and I_{TX} = 30 mA, PMOS driver fully on	TV_{DD} – 150	-	-	mV
$V_{OL,\ C32,\ 3\ V}$	LOW-level output voltage	TV_{DD} = 3.1 V and I_{TX} = 30 mA, NMOS driver fully on	-	-	200	mV

Table 56. Output resistance for TX1 and TX2

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{ON,01H}$	LOW-level output resistance	V_{TX} = TV_{DD} – 100 mV, CWGsN = 01h	-	-	60	Ω
$R_{ON,0FH}$	LOW-level output resistance	V_{TX} = TV_{DD} – 100 mV, CWGsN = 0Fh	-	-	4	Ω
R_{OP}	HIGH-level output resistance	V_{TX} = TV_{DD} – 100 mV	-	-	4	Ω

16. Package outline

VFBGA49: plastic very thin fine-pitch ball grid array package; 49 balls **SOT1320-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	max	1.00	0.25	0.75	0.35	4.1	4.4							
	nom	0.90	0.20	0.70	0.30	4.0	4.3	0.5	3.0	3.0	0.15	0.05	0.08	0.1
	min	0.80	0.15	0.65	0.25	3.9	4.2							

sot1320-1_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1320-1					~~11-11-11~~ 11-12-30

Fig 25. Package outline (Draft)

17. Abbreviations

Table 57. Abbreviations

Acronym	Description
AID	Application IDentifier
ASK	Amplitude Shift keying
Automatic anticollision	Detect and recognize requests from any NFC Initiator or Reader/Writer device, like NFC-Target, ISO/IEC 14443, Type A PICC (identical to NFC -Target) or ISO/IEC 14443, Type B PICC
Automatic device discovery	Detect and recognize any NFC peer devices (Initiator or target) like: NFC Initiator or target, ISO/IEC 14443-3, -4 Type A&B PICC, MIFARE Standard and Ultralight PICC, ISO/IEC 15693 VICC
Autonomous tag communication	Detect and recognize any NFC peer devices (Initiator or target) like: NFC Initiator or target, ISO/IEC 14443-3, -4 Type A&B PICC, MIFARE Standard and Ultralight PICC, ISO/IEC 15693 VICC
Card Emulation	The IC is capable of handling a PICC emulation on the RF interface including part of the protocol management. The application handling is done by the host controller.
Initiator	Generates RF field at 13.56 MHz and starts the NFCIP-1 communication.
Load modulation Index	The load modulation index is defined as the card's voltage ratio (Vmax - Vmin)/ (Vmax + Vmin) measured at the card's coil.
MISO	Master In Slave Out (for SPI interface)
Modulation Index	The modulation index is defined as the voltage ratio (Vmax – Vmin)/ (Vmax + Vmin).
MOSI	Master Out Slave In (for SPI interface)
NFC-WI	Near Field Communication - Wired Interface
NMOS	
NSS	Not Slave Select (for SPI interface)
PCD	Proximity Coupling Device. Definition for a Card reader/writer device according to the ISO/IEC 14443 specification or MIFARE.
PCD -> PICC	Communication flow between a PCD and a PICC according to the ISO/IEC 14443 specification or MIFARE.
PICC	Proximity Interface Coupling Card. Definition for a contactless Smart Card according to the ISO/IEC 14443 specification or MIFARE.
PICC-> PCD	Communication flow between a PICC and a PCD according to the ISO/IEC 14443 specification or MIFARE.
PMOS	
SCK	Serial Clock (for SPI interface)
SPI	Serial Peripheral Interface
Target	Responds to Initiator command either using load modulation scheme (RF field generated by Initiator) or using modulation of self generated RF field (no RF field generated by Initiator).
VCD	Vicinity Coupling Device. Definition for a reader/writer device according to the ISO/IEC 15693 specification.
VICC	
VGS	Voltage Gate Source

18. References

[1] **ETSI SWP** — TS 102 613 V9.2

[2] **ETSI HCI** — TS 102 622 V9.3

[3] **NFC Forum NCI** — NFC Controller Interface, version 1.0

[4] **NFC Forum DIGITAL** — Activity specification 1.0

[5] **NFC Forum ACTIVITY** — Digital protocol specification 1.0

[6] **ISO/IEC 14443** — parts 2: 2001 COR 1 2007 (01/11/2007), part 3: 2001 COR 1 2006 (01/09/2006) and part 4: second edition 2008 (15/07/2008)

[7] **I²C Specification** — I²C Specification, Version 2.1, January 2000, http://www.nxp.com/acrobat_download/literature/9398/39340011.pdf

[8] **SPI** — Motorola de-facto standard described in Motorola 68HC11 data sheet

[9] **PN547 User Manual** — UM10543 PN547 User Manual

[10] **PN547 Hardware Design Guide** — AN11163 PN547 Hardware Design Guide

[11] **PN547 Antenna Design Guide** — AN11164 PN547 Antenna Design Guide

[12] **ISO/IEC 18092 (NFC-IP1)** — first edition, 01/04/2004. This is similar to Ecma 340.

[13] **ISO/IEC15693** — part 2: second edition (15/12/2006), part 3: first edition (01/04/2001)

19. Revision history

Table 58. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
235830	20130701	Product data sheet	-	229614

Modifications:

- following changes are in this updated version:
  - pin name DL_REQ changed to DWL_REQ.
  - pin name SIM_SWIO changed to SWIO_UICC.
  - pin name SIM_VCC changed to SIMVCC.
  - pin name ESE_SWIO changed to SWIO_SE.
  - pin name HIF4 (I2C_SCL-SPI_SCK) changed to I2CSCL_SPISCK.
  - pin name HIF1 (I2C_ADR0-SPI_NSS changed to I2CADR0_SPINSS.
  - pin name HIF3 (I2C_SDA-SPI_MISO) changed to I2CSDA_SPIMISO.
  - pin name HIF2 (I2C_ADR1-SPI_MOSI) changed to I2CADR1_SPIMOSI.
  - pin name CLK1 changed to XTAL1.
  - pin name CLK2 changed to XTAL2.
- Section 2: Powered by the Field removed.
- Section 3: Powered by the Field removed.
- Table 1: row $I_{TVDDlim}$ with TV_{DD} = 2.7 V removed.
- Table 2: note 2 updated.
- Table 3: line 3, mask layout version removed.
- Section 10.1.1: Power by the Field removed.
- Section 10.5.3: Power by the Field removed.
- Section 10.6.1: PN547/C2 core supply sources removed.
- Section 10.6.1: VDHF part removed.
- Figure 11: VDHF part removed.
- Section 10.6.2: VDHF part removed.
- Section 10.6.3: All parts with TV_{DD} = 2.7 V removed.
- Figure 12: Line TV_{DD} = 2.7 V removed.
- Section 10.6.5: Power by the Field removed.
- Section 10.6.6: Power by the Field removed.
- Section 10.6.7: 220 mA at TV_{DD} = 2.7 V removed.
- Section 10.6.8: Powered by the Field mode (PbF) removed.
- Figure 16: updated.
- Figure 17: updated.
- Figure 18: updated.
- Figure 19: updated.
- Section 10.7.2.1: updated.
- Figure 22: updated.
- Table 28: line I_{SVDD}, Power by the Field removed.
- Table 39: updated.
- Table 45: note 1, Power by the Field removed.
- Table 46: note 1, Power by the Field removed.
- Table 55: line $V_{OH\_C32\_3\,V}$, TV_{DD} = 2.7 V removed.
- Table 55: line $V_{OL\_C32\_3\,V}$, TV_{DD} = 2.7 V removed.

Table 58. Revision history *...continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
235814	20130410	Objective data sheet	-	229613
235813	20130221	Objective data sheet		235812
235812	20121213	Objective data sheet		235811
235811	20120619	Objective data sheet		235810
235810	20120619	Objective data sheet		
Modifications:	• Initial version			

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Document status[1][2]	Product status[3]	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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